XN297 Datasheet

Single Chip 2.4GHz Transceiver

FEATURES

- Low Power

15mA at 0dBm output power TX mode, 14mA at RX mode, 2uA at Sleep mode.

- Low Cost

Few external elements, includes several chip R C L, and one crystal oscillator, good performance in two layer PCB, and can use PCB microstrip antenna, self-bring link layer communication protocol, easy to set to work.

- High Performance

-85dBm/-88dBm sensitivity at 2Mbps / 1Mbps, 11dBm at max output power, high linearity and selectivity, works well in complicated wireless environment.

APPLICATIONS

- Wireless Mouse, keyboards
- Set-top box remote controllers
- Wireless gamepads
- Toys
- Active RFID
- Smart home automation
- Wireless audio
- Security System

GENERAL DESCRIPTION

The XN297 is a single chip 2.4GHz transceiver which operates in 2.400~2483GHz worldwide use ISM frequency band. The XN297 integrates radio frequency (RF) transmitter and receiver, frequency synthesizer, oscillator driver, baseband GFSK modem, and so on. The XN297 also supports one -several network and communication with acknowledgement character (ack). The XN297 adjusts TX power, frequency channel, and data rate by SPI port.

2Mbps or 1Mbps data rate	Max to 8Mbps SPI exchange speed
32 byte or 64 byte payload length	QFN 20pin, side length 3mm package
16MHz oscillator ±60ppm	Operating voltage supply 2.1V~3.3V
GFSK	Auto ack reply and auto retransmission
Support RSSI detector	Data whitening and CRC

Version 1.3 2015.03

1 Electrical characteristics

Table1 XN297 Electrical characteristics

Symbol	Condition at VCC = 3V±5%, T=25℃	Parameter			Unit
		Min	Typ	Max	
ICC	Sleep		2		uA
	Standby I		50		uA
	Standby Ⅱ		750		uA
	TX at 0dBm output power		15	16	mA
	TX at 8dBm output power		23	25	mA
	RX at 2Mbps		15	16	mA
	RX at 1Mbps		14	15	mA
General RF					
f_{OP}	Operating frequency	2400		2483	MHz
PLL_{res}	PLL Programming resolution		1		MHz
f_{XTAL}	Crystal frequency		16		MHz
DR	Data rate	1		2	Mbps
Δf_{1M}	Frequency deviation at 1Mbps		160	250	KHz
Δf_{2M}	Frequency deviation at 2Mbps		320	500	KHz
FCH_{1M}	Channel spacing at 1Mbps		1		MHz
FCH_{2M}	Channel spacing at 2Mbps		2		MHz
Transmitter					
PRF	Typical output power 1		8		dBm
PRF	Typical output power 2		0		dBm
$PRFC$	Output Power Range	-11		11	dBm
$PBW2$	20dB Bandwidth for Modulated Carrier at 2Mbps		1.8	2.1	MHz
$PBW1$	20dB Bandwidth for Modulated Carrier at 1Mbps		0.9	1.1	MHz
Receiver					
$RX_{\max}$	Maximum received signal at <0.1% BER		0		dBm
$RXSENS2$	Sensitivity (0.1%BER) @2Mbps		-85		dBm

$RXSENS1$	Sensitivity (0.1%BER) @1Mbps		-88		dBm
C/I_{CO}	C/I Co-channel (@2Mbps)		13		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I		-8		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I		-12		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I		-20		dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I		-28		dBc
C/I_{CO}	C/I Co-channel (@1Mbps)		13		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I		5		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I		-10		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I		-16		dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I		-24		dBc
Operating conditions					
VDD	Supply voltage	2.1	3	3.3	V
VSS	Ground		0		V
V_{OH}	Output high level voltage	VDD-0.3		VDD	V
V_{OL}	Output low level voltage	VSS		VSS+0.3	V
V_{IH}	Input high level voltage	2.0	3	3.6	V
V_{IL}	Input low level voltage	VSS		VSS+0.3	V

2 Absolute maximum ratings

Table 2 XN297 absolute maximum ratings

Symbol	Condition	Parameter			Unit
		Min	Typ	Max	
maximum ratings					
V_{DD}	Supply voltage	-0.3		3.6	V

V_I	Input voltage	-0.3		5	V
V_O	Output voltage	VSS		VDD	
Pd	Total Power Dissipation (TA=-40℃~85℃)			100	mW
T_{OP}	Operating Temperature	-40		85	℃
T_{STG}	Storage Temperature	-40		125	℃

* Note: Exceeding one or more of the limiting values may cause permanent damage to XN297.

* Caution: Electrostatic sensitive device, comply with protection rules when operating.

3 Block diagram

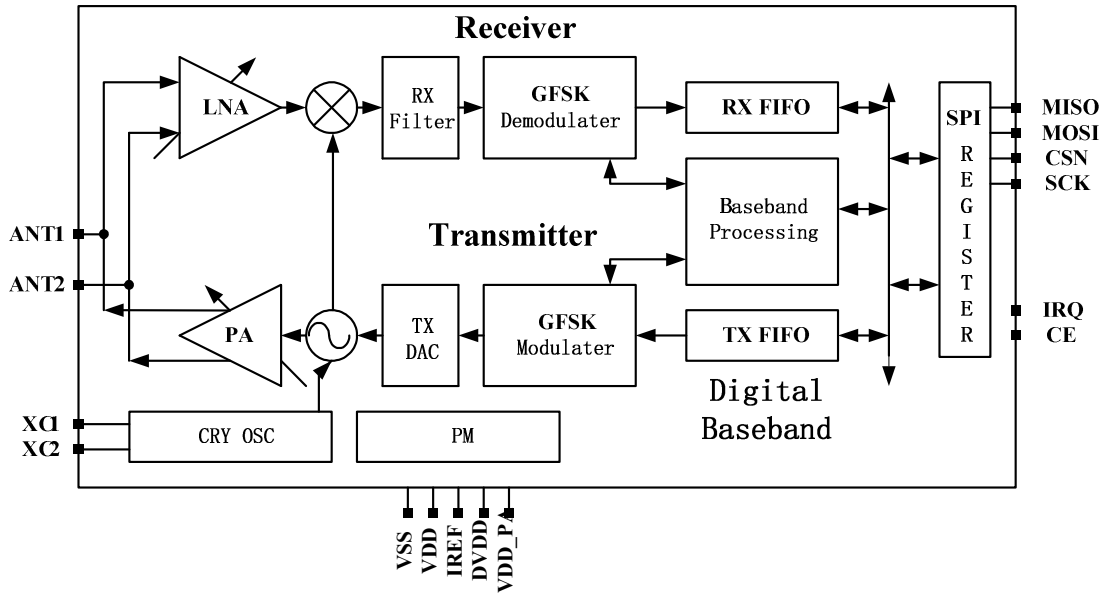


Figure 1 XN297 block diagram

4 Pin definition

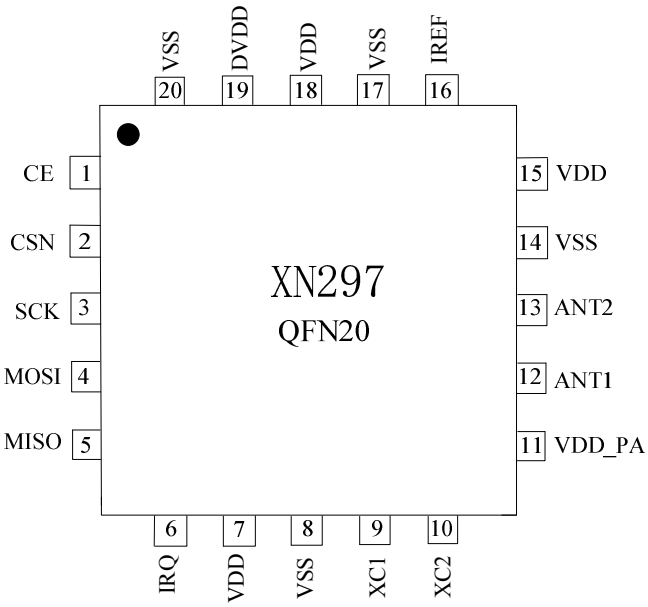


Figure2 XN297 pin definition

Table 3 Pin function

PIN	Name	Function	PIN	Name	Function
1	CE	Activates TX or RX mode	11	VDD_PA	Power Supply Output (+1.8V)
2	CSN	SPI Chip Select	12	ANT1	Antenna interface 1
3	SCK	SPI Clock	13	ANT2	Antenna interface 2
4	MOSI	SPI Data Input	14	VSS	Ground
5	MISO	SPI Data Output	15	VDD	Power Supply
6	IRQ	Interrupt pin	16	IREF	Reference current ouput
7	VDD	Power Supply	17	VSS	Ground
8	VSS	Ground	18	VDD	Power Supply
9	XC1	Crystal Pin 1	19	DVDD	Internal digital supply output
10	XC2	Crystal Pin 2	20	VSS	Ground

5 Operational modes

This chapter describes XN297 all kinds of working mode, and is used to control the chip into the working mode of method. XN297 own state machine is controlled by chip internal registers configuration values and external signal pin.

5.1 State diagram

Five kinds of working mode in table 4 gives the corresponding mode of control register and FIFO registers.

Table 4 Five kinds of working mode

MODE	PWR_UP BIT (CONFIG REG)	PRIM_RX BIT (CONFIG REG)	CE PIN	TX FIFO REG STATE
RX mode	1	1	1	X
TX mode	1	0	1	DATA IN TX FIFO
Standby I	1	X	0	X
Standby II	1	0	1	TX FIFO empty
SLEEP mode	0	X	X	X

5.2 State diagram

Figure 3 is XN297 working state diagram, said five working mode between jump XN297 in VDD is greater than 2.1 V to begin to work properly into sleep mode, the MCU can be sent via SPI configuration commands and CE pin into the other four state.

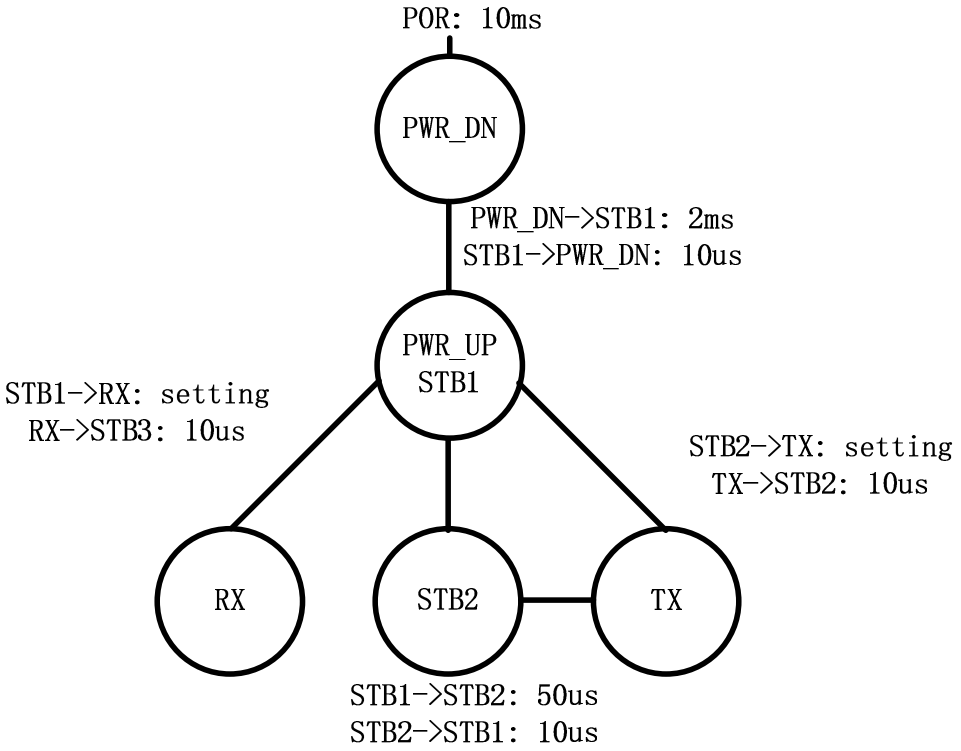


Figure3 state diagram

5.3 IRQ PIN

In the status register TX_DS RX_DR or MAX_RT is 1, report and the corresponding interrupt enable bit is 0, IRQ pins interrupt trigger. The MCU writes 1 to the corresponding interrupt source, clear the interrupt. IRQ pins interrupt trigger can be blocked or enabled, report by setting the interrupt enable bit is 1, ban IRQ pins interrupt triggered.

6 DATA FIFO

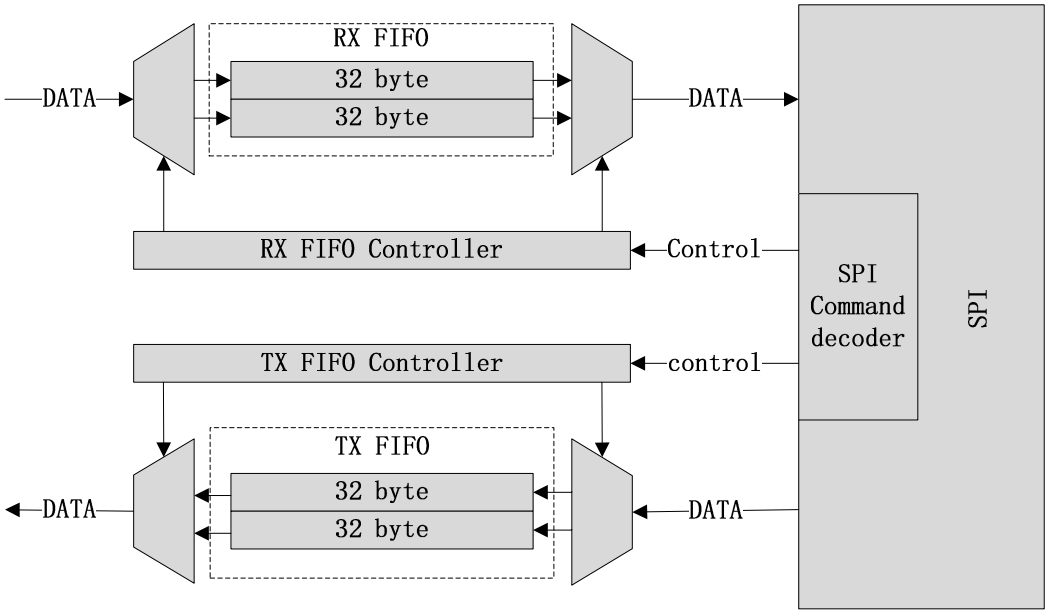


Figure 4 FIFO block diagram

The XN297 contains TX FIFO, RX FIFO. It is sent via SPI read/write command. It writes TX FIFO in TX mode by W_TX_PAYLOAD and W_TX_NO_ACK instructions. If MAX_RT interruption, data will not be cleared in the TX FIFO. It reads PAYLOAD in RX FIFO in receiving mode by R_RX_PAYLOAD, and it reads the length of the PAYLOAD by R_RX_PL_WID instruction. FIFO_STATUS register indicates FIFO states.

7 SPI control

The XN297 is controlled by SPI port for read and write register, and command. The XN297 is a slave terminal, SPI transfer rate depends on the MCU interface speed, and the maximum data transfer rate is 8 MBps.

SPI interface is a standard SPI interface are shown in table 5, you can use the general I/O for MCU simulation SPI interface. CSN pin to 0, SPI interface instructions to be performed. From 1 to 0 a CSN pin changes execute one instruction. After the change from 1 to 0 CSN pin can be read by MISO status

register contents.

Table 5 SPI port

PIN	I/O DIRECTION	FUNCTION DESCRIPTION
CSN	Input	SPI Chip Select
SCK	Input	Clock
MOSI	Input	Serial Data Input
MISO	Output	Serial Data Output

7.1 SPI commands

Table 6 SPI command format

<Command word: MSBit to LSBit (one byte)>

<Data bytes: LSByte to MSByte, MSBit in each byte first>

COMMAND	COMMAND WORD (BINARY)	DATA BYTES	OPERATION
R_REGISTER	000A AAAA	1 to 5	Read registers. AAAAA =5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5	Write registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32/64	Read RX-payload. A read operation starts at byte 0. Payload is deleted from RX FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32/64	Write TX-payload. A write operation starts at byte

			0. Used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode
REUSE_TX_PL	1110 0011	0	Used for a PTX device, reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH_TX is executed.
ACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: • R_RX_PL_WID • W_TX_PAYLOAD_NOACK A new ACTIVATE command with the same data deactivates them again. This is executable in power down or standby modes only.
R_RX_PL_WID	0110 0000	0	Read RX-payload width for the top, R_RX_PAYLOAD in the RX FIFO.
W_TX_PAYLOAD_NOACK	1011 0000	1 to 32/64	Write Payload to be transmitted, used in TX mode. Disable auto ACK on this packet.
NOP	1111 1111	0	No Operation.

The R_REGISTER and W_REGISTER commands can operate on single or multi-byte registers. When accessing multi-byte registers, first read or write the MSBit of LSByte. Terminate the writing before all bytes in a multi-byte register are written, then it leaves the unwritten MSByte(s) unchanged. For example, the LSByte

of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register.

7.2 SPI timing

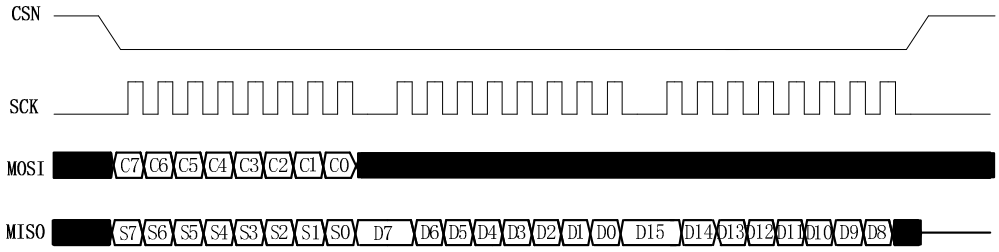


Figure 5 SPI read operation

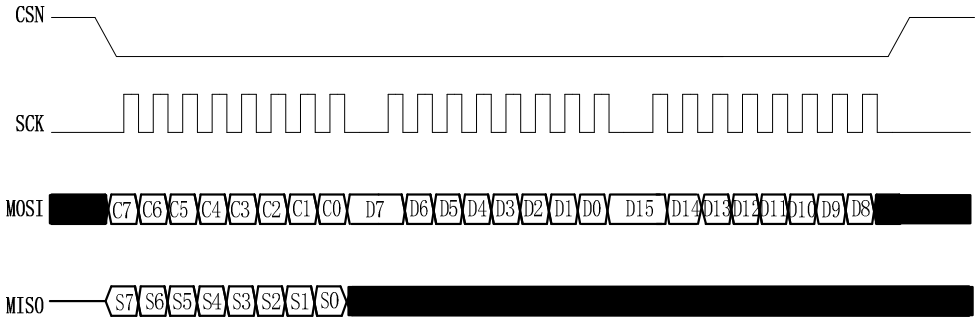


Figure 6 SPI write operation

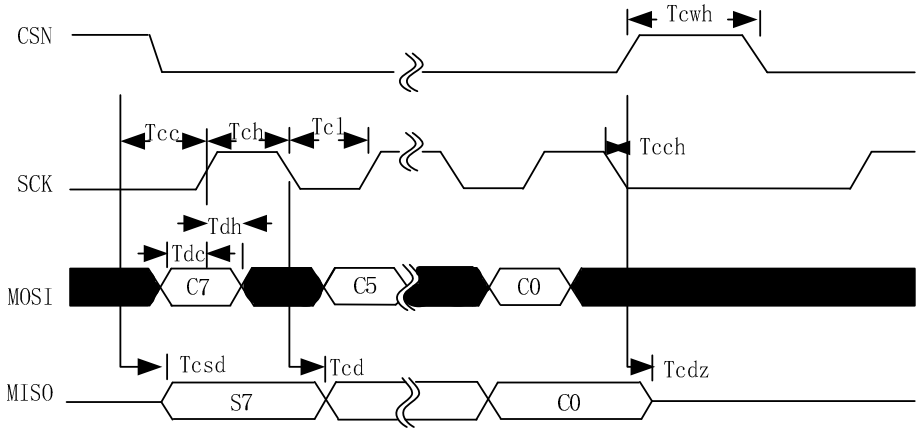


Figure 7 SPI NOP timing diagram

8 Packet format description

8.1 Packet format for normal Burst

Table 7 Packet format for normal burst

Preamble (3 byte)	Address (3~5 byte)	Payload (1~32/64 byte)	CRC (0/2 byte)

It can choose Address and Payload part to scramble, according to scrambler configuration bits.

8.2 Packet format for Enhanced Burst

Table 8 Packet format for enhanced burst

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			Payload (1~32/64 byte)	CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)		

It can choose Address, Package control field and Payload part to scramble, according to scrambler configuration bits.

8.3 Packet format for Enhanced Burst ACK

Table 9 Packet format for enhanced burst ack

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)	

It can choose Address, Package control field to scramble, according to scrambler configuration bits.

9 Application example

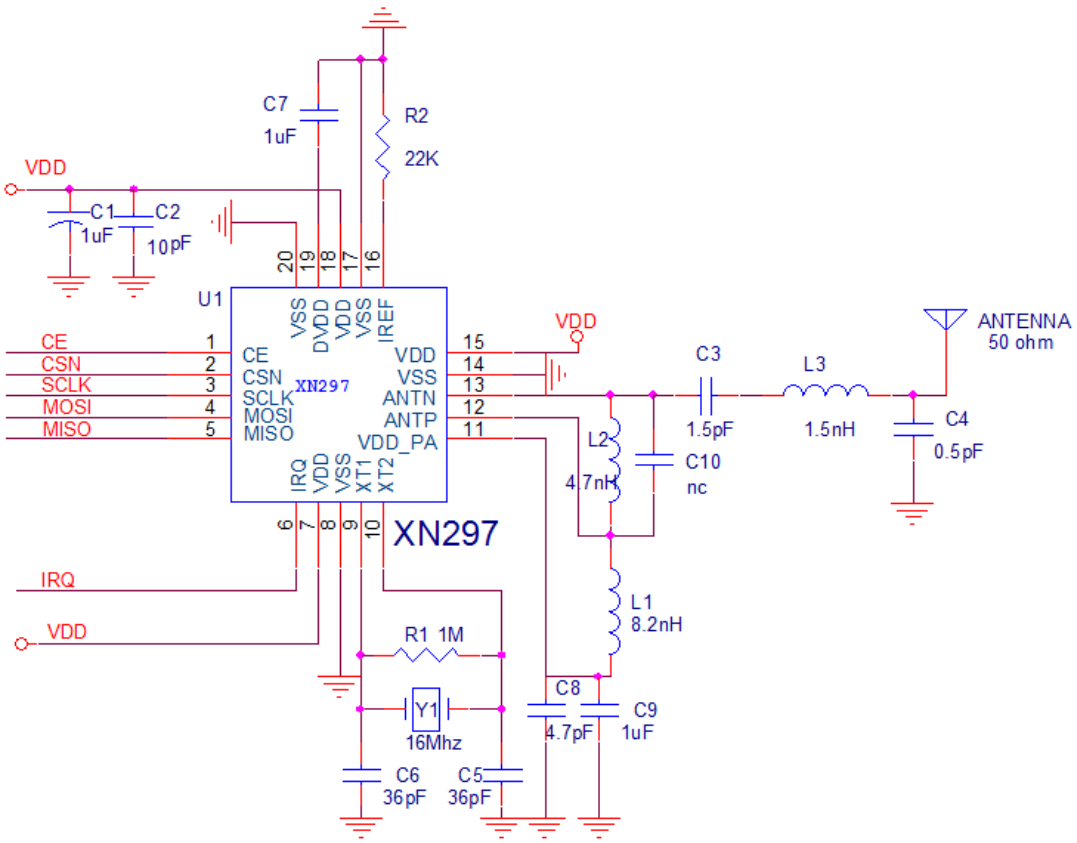
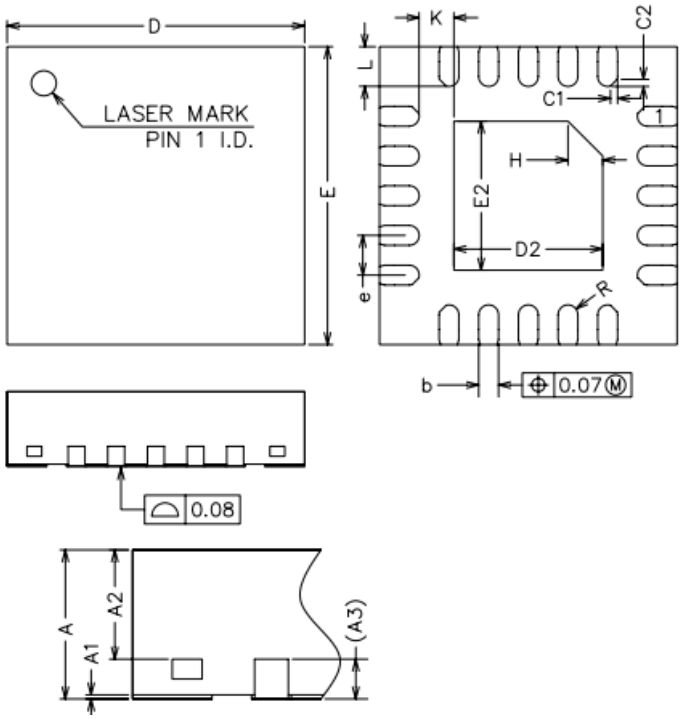


Figure 8 XN297 application

Note 1: nc means no welding device, reserved position.

Note 2: C5 / C6 crystals resonant capacitance need fine-tuning, according to the different types of crystals.

10 Package size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e	0.30	0.40	0.50
H		0.35REF	
K		0.35REF	
L	0.35	0.40	0.45
R	0.085	–	–
C1	–	0.07	–
C2	–	0.07	–

Figure 9 QFN20L 0303 package size