Panchip Microelectronics Co., Ltd.

PAN1026

User Manual

BLE Transceiver

Version: 1.9

Release date: Jun. 2023

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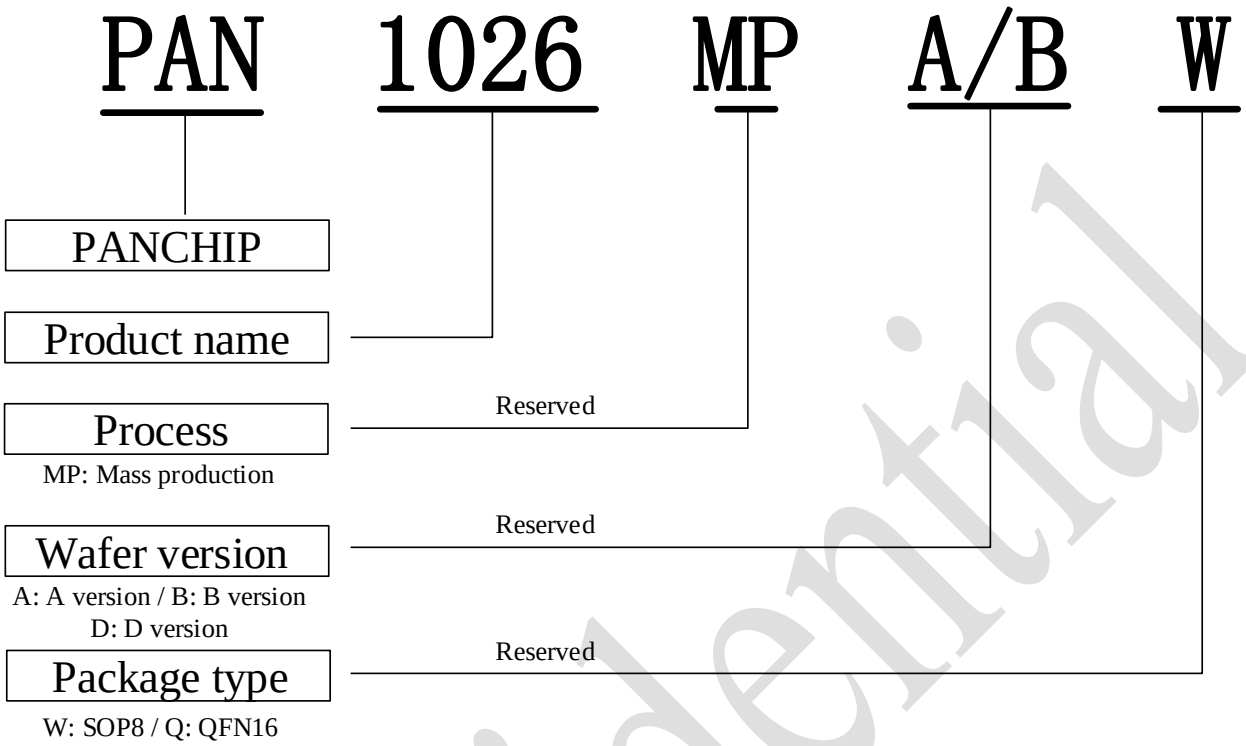
REVISION HISTORY

Version	Date	Content
1.0	Mar. 2021	Initial
1.1	Sep.2021	● Refresh the index of chapter "Electrical Characteristics" ● Refresh the package type ● Refresh Table 8-3 I2C Interface ● Refresh Naming Rules ● Refresh Product Series
1.2	Apr. 2022	Refresh the Application Reference Diagram
1.3	Aug. 2022	1. The transmit power is updated to a maximum of 10dBm 2. Add wafer version D 3. Add QFN16 package
1.4	Sep. 2022	Remove the Nordic nRF24L01
1.5	Oct. 2022	Update the pin definition for QFN16
1.6	Feb. 2023	1. Correct the STB2→STB3 time to 2ms in Figure 5-1 2. Add the "Controlled by CE" and update the STB2 parameter of the EN_LS in Table 5-1 3. Add description in Standby Mode-II(STB2).
1.7	May. 2023	Added the 250kbps data rate
1.8	May. 2023	Added the I2C function description of QFN16 in the Pin Description
1.9	Jun. 2023	Modify Figure 6-2 and its description; add reflow profile and MSL level

Naming Rules



Product Series

Product series	Wafer version	Package	Temperature
PAN1026MPAW	A	SOP8	-40℃~+85℃
PAN1026MPBW	B	SOP8	-40℃~+85℃
PAN1026MPDW	D	SOP8	-40℃~+85℃
PAN1026MPDQ	D	QFN16	-40℃~+85℃

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Abbreviation

ACK	Acknowledge Signal	MM	Machine Model
BLE	Bluetooth Low Energy	MOSI	Master Out Slave In
CDM	Charged Device Model	PLL	Phase Locked Loop
CRC	Cyclic Redundancy Check	PRX	Primary Receiver
DPLL	Digital Phase Locked Loop	PTX	Primary Transmitter
ESD	Electro-Static discharge	RC	Resistor-Capacitor Oscillator
FIFO	First Input First Output	RF	Radio Frequency
GFSK	Gauss frequency Shift Keying	RX	Receiver
HBM	Human-Body Model	SDA	Serial Data
I2C	Inter Integrated-Circuit	SPI	Serial Peripheral Interface
LDO	Low Dropout Regulator	STB	Standby Mode
MCU	Microcontroller Unit	TX	Transmitter
MISO	Master In Slave Out	XTAL	External Crystal

1 General Description

PAN1026 is a low-cost, highly integrated BLE transceiver that works in the ISM frequency band of 2400MHz ~ 2483MHz. PAN1026 has low cost of system application because it only needs one MCU and a few external passive components to build a system to meet the requirements of wireless applications. Moreover, the use of PAN1026 is very convenient. It only needs the MCU to configure a few registers of the chip by the SPI/I2C to transmit and receive data.

The PAN1026 integrates transmitter, receiver, frequency generator, and GFSK modem. The transmitter power is adjustable (up to 10dBm). The receiver adopts a digital communication mechanism and has good performance of receiving and transmission in complex environments with strong interference.

The frame structure of PAN1026 is compatible with XN297L and BLE data packets. The package of PAN1026 is compatible with XN297L (SOP8, 3-wire SPI function).

1.1 Key Features

- **RF**
  - Radio
    - Frequency band: 2.400 ~ 2.483GHz
    - Data rate: 2Mbps, 1Mbps, 250kbps
    - Modulation: GFSK
    - Compatibility: compatible with XN297L (SOP8, 3-wire SPI function)
  - RF Synthesizer
    - Fully integrated synthesizer
    - Accept low cost ±10ppm crystal oscillator for the data rate of 250kbps
    - Accept low cost ±40ppm crystal oscillator for the data rate of 1Mbps and 2Mbps
  - Transmitter
    - Transmitter output power is up to 10dBm
    - 25mA @0dBm
  - Receiver
    - -88dBm@1Mbps
    - Work mode current: 20mA
    - DEEP_SLEEP mode current: 0.1uA
  - Protocol Engine
    - Support up to 64 bytes payload data
    - Support automatic retransmission and ACK
    - 6 receiving channels form a 1:6 star network
- **Power Management**
  - Integrated voltage regulator
  - Operating voltage range: 2.2 to 3.6V
- **Host Interface**
  - Support 4-wire/3-wire SPI and 2-wire I2C

- Up to 16Mbps SPI interface rate
- Up to 1.5Mbps I2C interface rate
- Support two independent 32-byte TX and RX FIFOs
- Support one 64-byte TX and RX FIFOs

- **Package**
  - SOP8
  - QFN16
- **DC/AC Characteristics**
  - Operating Temperature: -40 ~ +85℃(-40 ~ +70℃ @250kbps)
- **Other Features**
  - ESD
    - HBM: ±2KV
    - MM: ±100V
    - CDM: ±2KV
  - Support Automatic scrambling and CRC check
  - Support white list filtering of BLE mode
  - Fewer external components

1.2 Typical Applications

- Smart home
- Remote control

2 Block Diagram

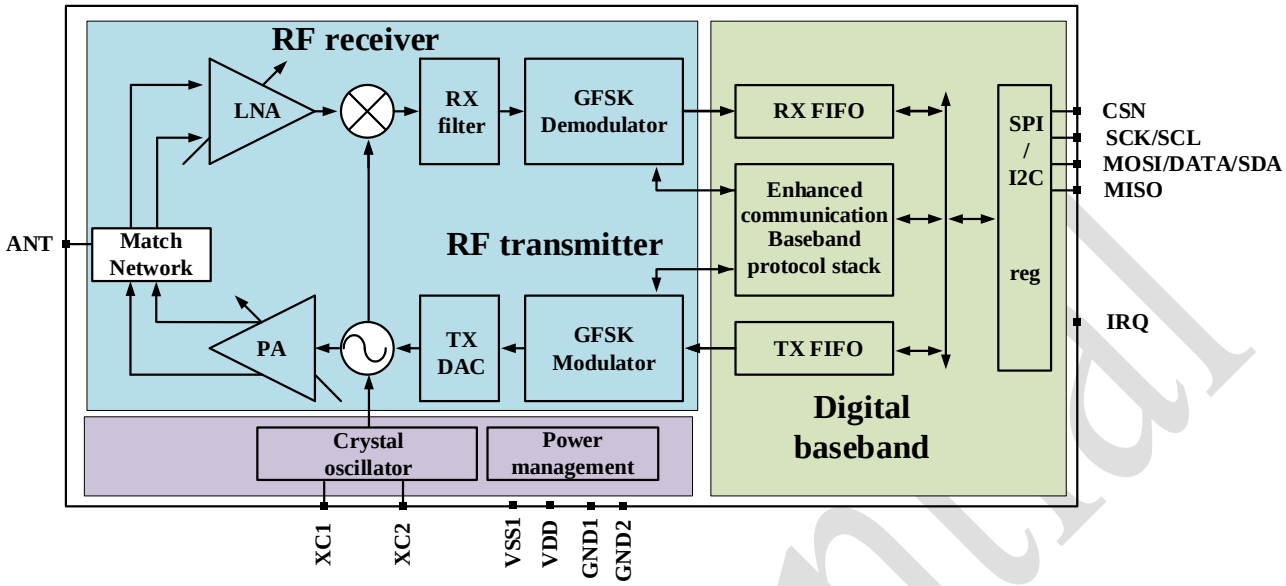


Figure 2-1 Block Diagram

3 Pin Information

3.1 Pin Diagram

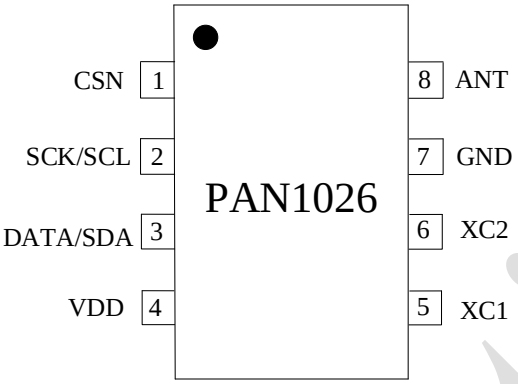


Figure 3-1 SOP8 Diagram

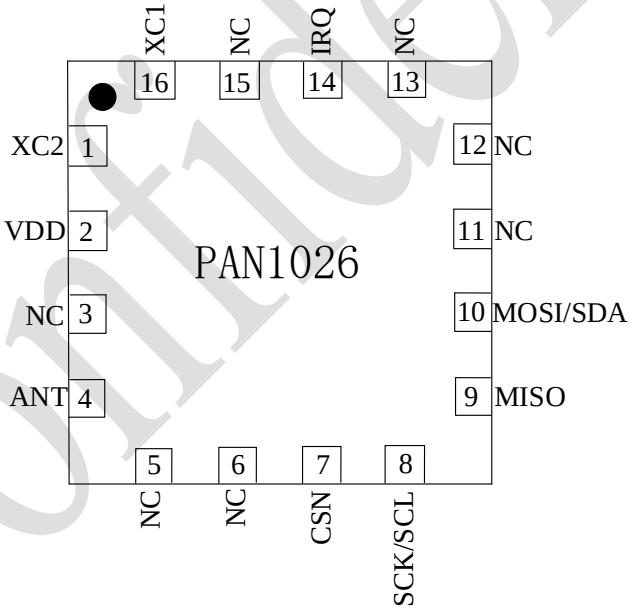


Figure 3-2 QFN16 Diagram

3.2 Pin Description

Table 3-1 SOP8 Pin Descriptions

No.	Symbol	I/O	Function
1	CSN	I	The chip select signal of SPI
2	SCK	I	The clock signal of SPI
	SCL	I	The clock signal of I2C
3	DATA	I/O	The data input/output of 3-wire SPI
	SDA	I/O	The data input/output of I2C
4	VDD	P	Power supply input (2.2~3.6V DC)
5	XC1	AI	Crystal oscillator input
6	XC2	AO	Crystal oscillator output
7	GND	G	Ground (GND)
8	ANT	AI	Antenna interface

Table 3-2 QFN16 Pin Descriptions

序号	符号	类型	功能
1	XC2	AO	Crystal oscillator output
2	VDD	P	Power supply input (2.2~3.6V DC)
3	NC	-	-
4	ANT	AI	Antenna interface
5	NC	-	-
6	NC	-	-
7	CSN	I	The chip select signal of SPI
8	SCK	I	The clock signal of SPI
	SCL	I	The clock signal of I2C
9	MISO	I/O	SPI data output signal
10	MOSI	I/O	SPI data input signal
	SDA	I/O	The data input/output of I2C
11	NC	-	-
12	NC	-	-
13	NC	-	-
14	IRQ	I/O	Interrupt signal
15	NC	-	-
16	XC1	AI	Crystal oscillator input

4 Electrical Characteristics

Conditions: VCC = 3.0V±5%, TA=25℃

4.1 DC Electrical Characteristics

Table 4-1 DC characteristics

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
VDD	Power supply voltage	2.2	3.0	3.6	V
VSS	Ground	-	0	-	V
VOH	Output high voltage	VDD-0.3	-	VDD	V
VOL	Output low voltage	VSS	-	VSS+0.3	V
VIH	Input high voltage	VDD-0.3	-	VDD	V
VIL	Input low voltage	VSS	-	VSS+0.3	V

Note: Exceeding one or more maximum ratings may cause permanent damage to PAN1026.

4.2 Absolute Maximum Ratings

Table 4-2 Absolute Maximum Ratings

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
VDD	Power supply voltage	-0.3	-	3.6	V
V_I	Input voltage	-0.3	-	3.6	V
V_O	Output voltage	VSS	-	VDD	-
Pd	Total power consumption (temperature=-40℃~85℃)	-	250	-	mW
T_{OP}	Operating Temperature	-40	-	85	℃
T_{STG}	Storage Temperature	-40	-	125	℃

4.3 Current Consumption

Table 4-3 Current Parameter

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
I_{CC}	DEEP_SLEEP mode	-	100	-	nA
	Standby mode -I	-	170	-	uA
	Standby mode -III	-	460	-	uA
	Standby mode-II	-	225	-	uA
	TX mode@ -40dBm output power	-	13	-	mA
	TX mode@ -30dBm output power	-	15	-	mA
	TX mode@ -27dBm output power	-	20	-	mA
	TX mode@ -10dBm output power	-	23	-	mA

	TX mode@ 0dBm output power	-	25	-	mA
	TX mode@ 2dBm output power	-	28	-	mA
	TX mode@ 8dBm output power	-	52	-	mA
	TX mode@ 10dBm output power	-	57	-	mA
	RX mode@ 2Mbps	-	20	-	mA
	RX mode@ 1Mbps	-	20	-	mA
	RX mode@ 250kbps	-	20	-	mA

4.4 RF Parameter

Table 4-4 RF Parameter

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
f_{OP}	Working frequency band	2400	-	2483	MHz
PLL_{res}	PLL programming resolution	-	1	-	MHz
f_{XTAL}	Crystal frequency	-	16	-	MHz
DR	Data rate	1	-	2	Mbps
Δf_{250K}	Frequency deviation at 250kbps	-	150	180	kHz
Δf_{1M}	Frequency deviation at 1Mbps	-	250	300	kHz
Δf_{2M}	Frequency deviation at 2Mbps	-	500	600	kHz
FCH_{250K}	Channel Spacing at 250kbps	-	1	-	MHz
FCH_{1M}	Channel Spacing at 1Mbps	-	1	-	MHz
FCH_{2M}	Channel Spacing at 2Mbps	-	2	-	MHz

Note: It is not recommended to use channels with integer multiples of 16MHz, such as 2480MHz. Because the sensitivity of the receiver will be reduced by about 2dB in these channels.

4.5 TX Parameter

Table 4-5 TX Parameter

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
P_{RF}	Maximum output power	-	8	10	dBm
P_{RFC}	RF power control range	-40	-	10	dBm

4.6 RX Parameter

Table 4-6 RX Parameter

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
RX_{max}	Maximum receiving amplitude when bit error rate <0.1%	-	0	-	dBm
RXSENS1	Receiving sensitivity (0.1%BER) @2Mbps	-	-84	-	dBm
RXSENS2	Receiving sensitivity (0.1%BER) @1Mbps	-	-88	-	dBm
$RXSENS3$	Receiving sensitivity (0.1%BER) @250kbps	-	-96	-	dBm

C/I_{CO}	C/I Co-channel (@2Mbps)	-	13	-	dBc
C/I_{1ST}	The 1st adjacent channel selectivity C/I	-	18	-	dBc
C/I_{2ND}	The 2nd adjacent channel selectivity C/I	-	-15	-	dBc
C/I_{3RD}	The 3rd adjacent channel selectivity C/I	-	-17	-	dBc
C/I_{4TH}	The 4th adjacent channel selectivity C/I	-	-21	-	dBc
C/I_{5TH}	The 5th adjacent channel selectivity C/I	-	-25	-	dBc
C/I_{CO}	C/I Co-channel (@1Mbps)	-	12	-	dBc
C/I_{1ST}	The 1st adjacent channel selectivity C/I	-	0	-	dBc
C/I_{2ND}	The 2nd adjacent channel selectivity C/I	-	-32	-	dBc
C/I_{3RD}	The 3rd adjacent channel selectivity C/I	-	-28	-	dBc
C/I_{4TH}	The 4th adjacent channel selectivity C/I	-	-31	-	dBc
C/I_{5TH}	The 5th adjacent channel selectivity C/I	-	-34	-	dBc
C/I_{6TH}	The 6th adjacent channel selectivity C/I	-	-37	-	dBc

5 Chip Working Status

This chapter describes various working modes of the PAN1026 and the methods that control the chip to enter each working mode. PAN1026's state machine is controlled by the configuration value of the internal registers and external pin signals.

Figure 5-1 is a working state diagram of PAN1026 which shows transition between the five working modes. PAN1026 starts to work when VDD is greater than 2.2V. MCU can still send configuration commands by SPI to enter the other five states even in DEEP_SLEEP mode.

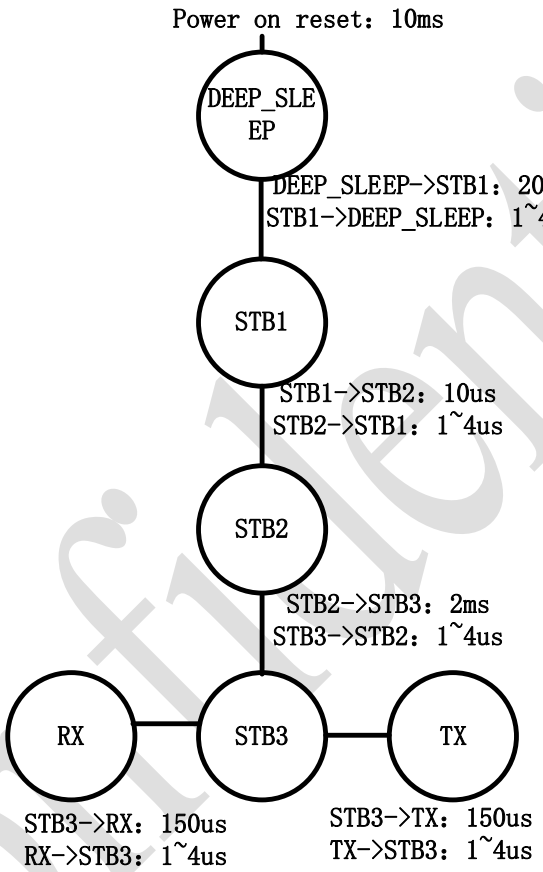


Figure 5-1 Working Status Diagram

Table 5-1 Control Signal and Functional Description

Status	DEEP_SLEEP	STB1	STB2	STB3	RX	TX
Control signal						
EN_PM	0	1	1	1	1	1
EN_LDO_DVDD	0	0	1	1	1	1
EN_LS	0	0	1	1	1	1
PWR_UP	0	0	0	1	1	1
EN_CLK_BUF(Controlled by CE)	X	X	X	0	1	1
EN_LDO_1P8V(Controlled by CE)	X	X	X	0	1	1

PRIM_RX	X	X	X	0	1	0
Functional description						
3V SPI operation	√	√	√	√	√	√
3V reg value storage	√	√	√	√	√	√
1.8V SPI operation	X	X	X	√	√	√
1.8V reg value storage	X	X	X	√	√	√
Bandgap, current source enabled	X	√	√	√	√	√
DVDD LDO enabled	X	X	√	√	√	√
Crystal oscillator start-up	X	X	X	√	√	√
Crystal oscillator output	X	X	X	X	√	√
TX module enabled	X	X	X	X	X	√
RX module enabled	X	X	X	X	√	X

5.1 DEEP_SLEEP Mode

In DEEP_SLEEP mode, all the functions of PAN1026 are turned off except 3V area to keep the minimum current consumption. After entering the DEEP_SLEEP mode, PAN1026 stops working, but keeps the configuration of 3V register. The DEEP_SLEEP mode is controlled by the PWR_UP, EN_LS, EN_LDO_DVDD, EN_PM bits in the 3V register.

5.2 Standby Mode-I(STB1)

In standby mode-I, all the function are turned off except bandgap and current source to ensure small current consumption. In DEEP_SLEEP mode, the chip can enter the standby mode -I by configuring the value of the EN_PM register. When in receive mode or transmit mode, the system returns STB1 by setting PWR_UP, EN_LS, EN_LDO_DVDD to 0.

5.3 Standby Mode-II(STB2)

The chip transfers from STB1 to STB2 by configuring EN_LDO_DVDD to 1. STB2 is mainly designed to ensure that the output of DVDD LDO is ahead of XTAL oscillator output, and in STB2, 1.8V register data can be maintained.

Note: To operate the 1.8V register, the DVDD LDO must be turned on. The crystal oscillator can be turned on as needed.

5.4 Standby Mode-III(STB3)

By configuring PWR_UP to 1, the chip enters STB3 from STB2. And the crystal oscillator is enabled.The chip returns to TX or RX mode from standby mode-III by configuring PRIM-RX, SPI_CE and operating FIFO.

5.5 Receive Mode (RX)

When PWR_UP, PRIM-RX, EN_PM, SPI_CE are set to 1, the chip enters the receive mode.

In RX mode, the RF part receives, amplifies, down-converts, filters and demodulates the signal from the antenna. The validity of the received packet is judged according to the address, CRC and data length. The valid packet will be uploaded to the RX FIFO and the interruption will be reported. If the RX FIFO is full, the received packet will be discarded.

5.6 Transmit Mode (TX)

To enter TX mode, PWR_UP, EN_PM, SPI_CE should be set to 1, PRIM_RX should be 0 and valid data should be in TX FIFO.

PAN1026 will remain in TX mode until the data packet transmission completes. Once transmission completes, the chip will return standby mode. PAN1026 adopts PLL open-loop transmission, and single packet transmission is adopted.

6 Data Communication Mode

Communication is completed by PAN1026 and MCU. At the link layer, processing such as data framing, verification, address judgment, data whitening scrambling code, data retransmission and ACK response is completed inside the chip without MCU.

The PAN1026 can be configured as two different RX FIFO registers (32 bytes) or one RX FIFO register (64 bytes) (shared by 6 receiving channels), two different TX FIFO registers (32 bytes) or one TX FIFO register (64 bytes). In DEEP_SLEEP mode and standby mode, MCU can access the FIFO register.

PAN1026 has two data communication modes:

- The communication mode without automatic retransmission and ACK (normal mode): the transmitter can use commands such as W_TX_PAYLOAD, REUSE_TX_PL, etc.
- The communication mode with automatic retransmission and ACK (enhanced mode): the transmitter can use commands such as W_TX_PAYLOAD, W_TX_PAYLOAD_NOACK, REUSE_TX_PL. The receiver can use commands such as W_ACK_PAYLOAD, etc.

Table 6-1 Normal Mode

Communication name	**Normal mode**	
Communication	PTX	PRX
Feature	One-way transmission	One-way receive
The framing method of transmitting data	I	-
Turn on the REUSE_TX_PL command	Retransmit the previous packet of data	-

Table 6-2 Enhanced Mode

Communication name	**Enhanced mode**	
Communication	PTX	PRX
Feature	After transmitting data, waiting to receive ACK	After receiving the data, transmitting ACK
The framing method of transmitting data	Transmitting data	Transmitting ACK
PTX uses the REUSE_TX_PL command	Repeating the previous packet of data	Transmitting ACK after receiving a packet every time

PTX uses W_TX_PAYLOAD command PRX uses the W_ACK_PAYLOAD command	After sending data, waiting to receive ACK PAYLOAD	After receiving the data, transmitting ACK PAYLOAD
PTX uses W_TX_PAYLOAD_NO ACK command	Transmitting data once without waiting for ACK	Receiving data without Transmitting ACK

6.1 Normal Mode

In normal mode, transmitter gets and transmits data from TX FIFO register. Once the transmission completes, an interrupt will be reported and then be cleared. Meanwhile, TX FIFO is cleared. Receiver will upload interrupt and inform MCU if receives valid address and data. MCU reads data from RX FIFO. (RX FIFO and RX FIFO should be emptied. Interrupt should be cleared.)

In the normal mode, (0x01) EN_AA register is set to 0x00, (0x04) SETUP_RETR register is set to 0x00, (0x1C) DYNPD register is set to 0x00, (0x1D) FEATURE register's lowest 3 bits are set to 000.

6.2 Enhanced Mode

In the enhanced mode, PTX (Primary Transmitter) initiates communication and PRX (Primary Receiver) receives data and responds. The PTX waits for ACK after sending the data, and the PRX responds ACK after receiving the valid data. If PTX does not receive the ACK within the specified time, it will automatically retransmit the data. PAN1026 can automatically retransmit and respond without MCU.

PTX automatically switches to RX mode after sending data and waits for ACK. If the correct response signal is not received within the specified time, PTX will retransmit the same data packet until the correct response signal is received. If the number of retransmission exceeds the value of ARC (SETUP_RETR register), interrupt MAX_RT will be generated. PTX receives the response signal, which means that the data has been sent successfully (PRX receives valid data). Then it clears the data in the TX FIFO and generates a TX_DS interrupt (TX FIFO and RX FIFO need to be cleared, and the interrupt needs to be cleared).

PRX will respond ACK signal every time , if it receives a packet of valid data. If the data is new data (the PID value is different from the previous packet data), it will be saved to the RX FIFO, otherwise it will be discarded.

In the enhanced mode, it is necessary to ensure that the TX address of PTX (TX_ADDR), the RX address of channel 0 (such as RX_ADDR_P0), and the RX address of PRX (such as RX_ADDR_P5) are the same. For example: in Figure 6-3, PTX5 corresponds to data channel 5 of PRX, and the address is set as follows:

PTX5: TX_ADDR=0xC2C3C4C5C1

PTX5: RX_ADDR_P0=0xC2C3C4C5C1

RX: RX_ADDR_P5=0xC2C3C4C5C1

The enhanced mode has the following characteristics:

- Reducing the participation of MCU and software.
- Reducing packet loss caused by instantaneous co-frequency interference in wireless transmission and making it easier to develop frequency hopping algorithms.

- Reducing the operation time for MCU to write the data to be sent by the SPI interface during retransmission.

6.3 Enhanced Transmission Mode

1. Set SPI_CE to 0 and set the PRIM_RX bit of the CONFIG register to 0.

2. When sending data, the transmission address (TX_ADDR) and valid data (TX_PLD) are written into the address register and TX FIFO in bytes by the SPI interface. When CSN pin is low, data are written in. When CSN pin is high, data writing is finished.

3. When SPI_CE is set to 1, the transmission starts (The signal CE should keep high for at least 30 us to ensure the effectiveness of the operation.).

4. In automatic response mode (SETUP_RETR register is not set to 0, ENAA_P0 =1), PTX will automatically switch channel 0 to RX mode and wait for the response signal immediately after sending the data. If the ACK signal is received within the valid response time, the data transmission is successful. Then the TX_DS bit of the status register will be set to 1 and the data in the TX FIFO will be automatically cleared. If no response signal is received within the setting time, the data will be automatically retransmitted.

5. If the automatic transmission counter (ARC_CNT) overflows (exceeds the set value), the MAX_RT bit of the status register will be set to 1 and the data in the TX FIFO will not be cleared. When MAX_RT or TX_DS is 1, the IRQ pin generates a low-level interrupt (The corresponding interrupt needs to be enabled.). The interrupt can be reset by writing the status register.

6. The packet loss counter (PLOS_CNT) is incremented by one after generation of each MAX_RT interrupt. The automatic transmission counter ARC_CNT counts the number of retransmissions of data packets. The data packet loss counter PLOS_CNT counts the number of data packets that have not been successfully sent when the maximum allowable number of transmission is reached.

7. After the generation of MAX_RT or TX_DS interrupt, the system enters standby mode.

6.4 Enhanced Receiving Mode

1. SPI_CE is set to 0 and the PRIM_RX bit of the CONFIG register is set to 1. The channel ready to receive data must be enabled (EN_RXADDR register). The automatic response function of all data channels that work in enhanced communication mode is enabled by the EN_AA register. The valid data width is set by the RX_PW_PX register.

2. The receiving mode starts by setting SPI_CE to 1.

3. After the preset waiting time, PRX starts to detect wireless signals.

4. After receiving a valid data packet, the data will be stored in RX_FIFO and the RX_DR bit will be set to 1, then an interrupt is generated. The RX_P_NO bit in the status register shows which channel the data is received.

5. Automatically transmit ACK signal.

6. If SPI_CE remains at high level, the chip will remain in receiving mode. If SPI_CE is set to 0, the chip will switch to the standby mode-III.

7. The MCU reads the data by SPI at the appropriate rate.

6.5 Data Packet Recognition in Enhanced Mode

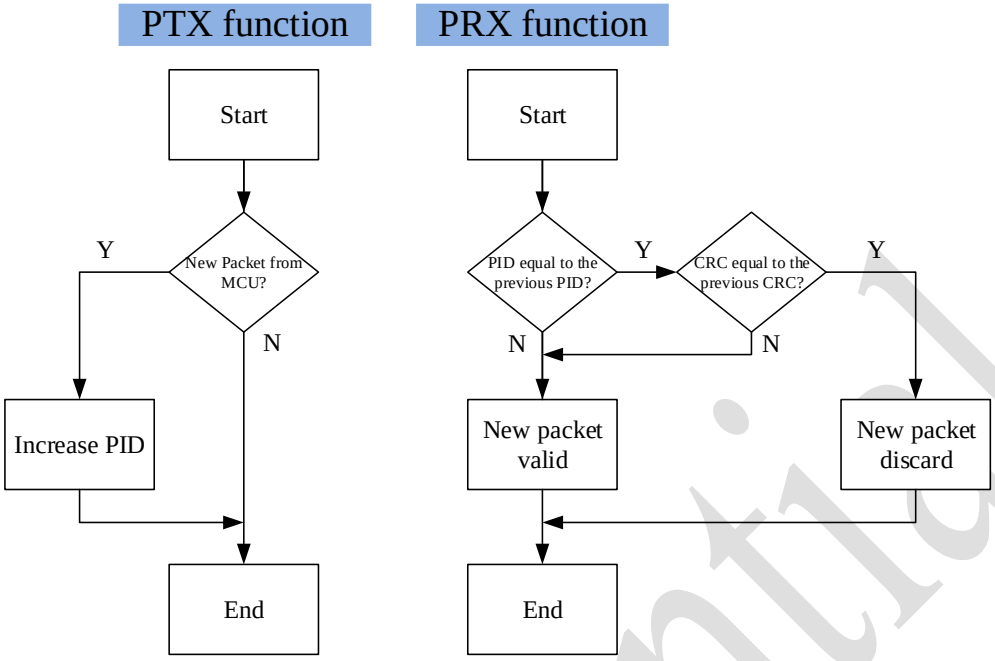


Figure 6-1 PID Generation and Detection

Each packet of data includes a two-bit PID (data packet flag) to help the receiver identify whether the data is a new packet or a retransmitted packet to prevent multiple storage of the same packet. PID generation and detection is shown in Figure 6-1. When the receiver terminal obtains a packet of new data from the MCU, the PID value will increase by one.

6.6 Timing diagram of PTX and PRX in enhanced mode

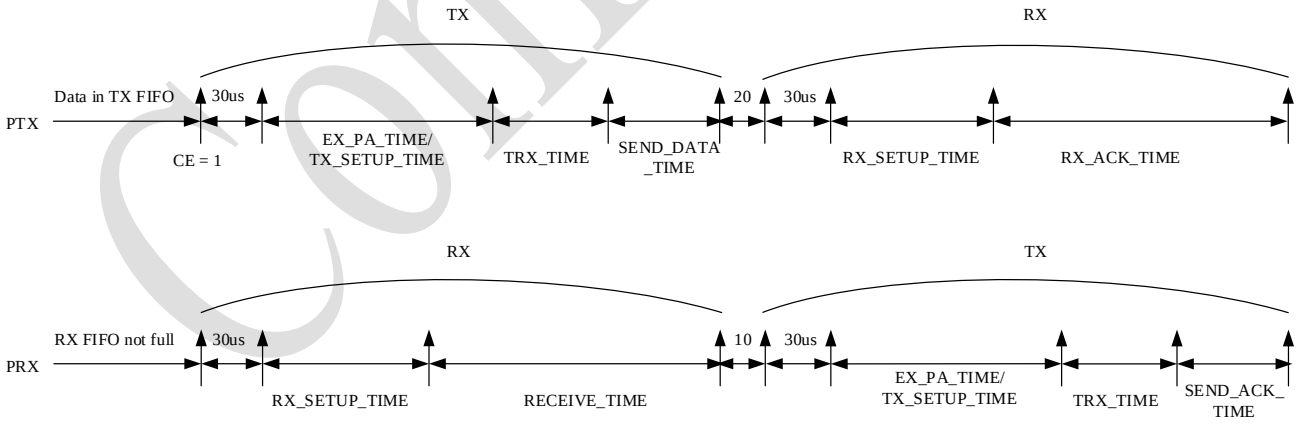


Figure 6-2 Timing diagram of PTX and PRX in enhanced mode (send successfully)

The internal timing diagram of the communication between PTX and PRX is shown in Figure 6-2. The following two conditions must be met to make the communication successful:

Condition 1:

max(EX_PA_TIME，TX_SETUP_TIME) + TRX_TIME > RX_SETUP_TIME +20us

Condition 2:

max(EX_PA_TIME，TX_SETUP_TIME) + TRX_TIME + SEND_ACK_TIME <

RX_SETUP_TIME + RX_ACK_TIME - 80us

6.7 One-to-many Communication at the RX Terminal in Enhanced Mode

As a transmitter, PAN1026 can use different addresses to communicate with multiple receivers in one-to-many communication.

As a receiver, PAN1026 can receive data from transmitters with 6 different address and the same frequency. Each data channel has its own address.

Data channels are enabled by register EN_RXADDR. The address of each data channel is configured by the register RX_ADDR_PX. Normally, different data channels are not allowed to set the same address. As follows, Table 6-3 gives an example of multiple receiving channel address configuration.

Table 6-3 Multiple Channel Address Setting

	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Data pipe 0(RX_ADDR_P0)	0xF1	0xD2	0xE6	0xA2	0x33
Data pipe 1(RX_ADDR_P1)	0xD3	0xD3	0xD3	0xD3	0xD3
Data pipe 2(RX_ADDR_P2)	0xD3	0xD3	0xD3	0xD3	0xD4
Data pipe 3(RX_ADDR_P3)	0xD3	0xD3	0xD3	0xD3	0xD5
Data pipe 4(RX_ADDR_P4)	0xD3	0xD3	0xD3	0xD3	0xD6
Data pipe 5(RX_ADDR_P5)	0xD3	0xD3	0xD3	0xD3	0xD7

It is shown in Table 6-3 that the 5-byte address (40 bits) of data channel 0 is configurable. The address of data channel 1~5 is configured as a 32-bit shared address (shared with channel data 1) + 8 bits of the channel's own address (The lowest byte). The PAN1026 can communicate with up to 6 different channels in the receiving mode, as shown in Figure 6-3. Each data channel uses different address and shares the same channel. All the transmitters and receivers are set to enhanced mode.

The PRX records the TX address of the PTX after receiving the valid data and transmits a response signal to this address. When PTX data channel 0 is used to receive the response signal, the RX address of data channel 0 must be equal to the TX address to ensure that the correct response signal is received.

Figure 6-3 shows an example to configure PTX and PRX addresses.

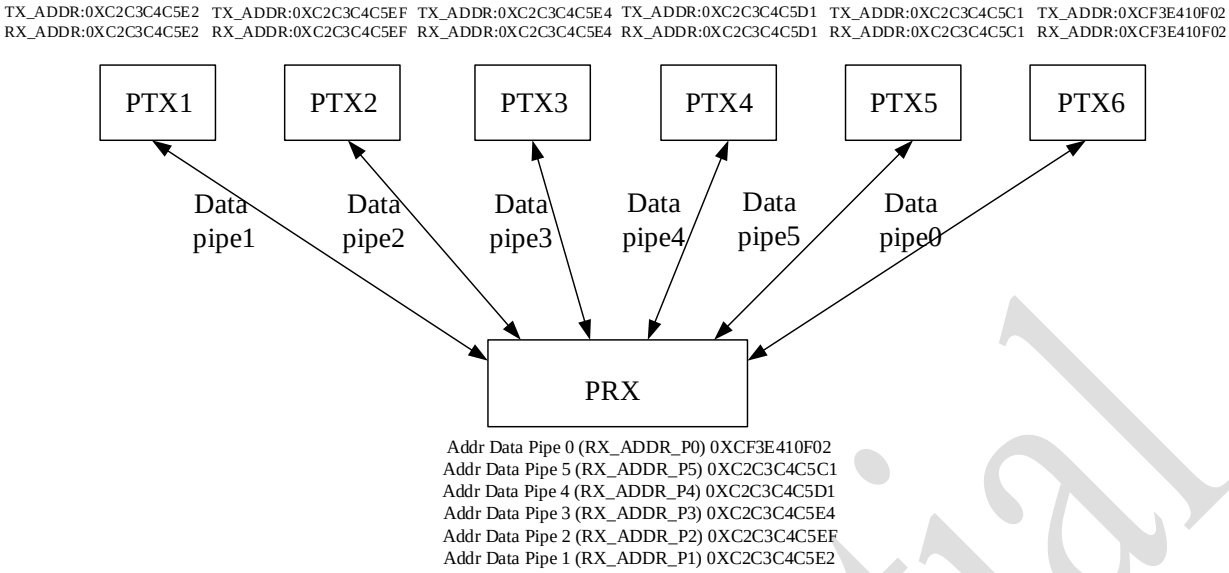


Figure 6-3 Example of Data Pipe Addressing Under Star Network

6.8 Data FIFO

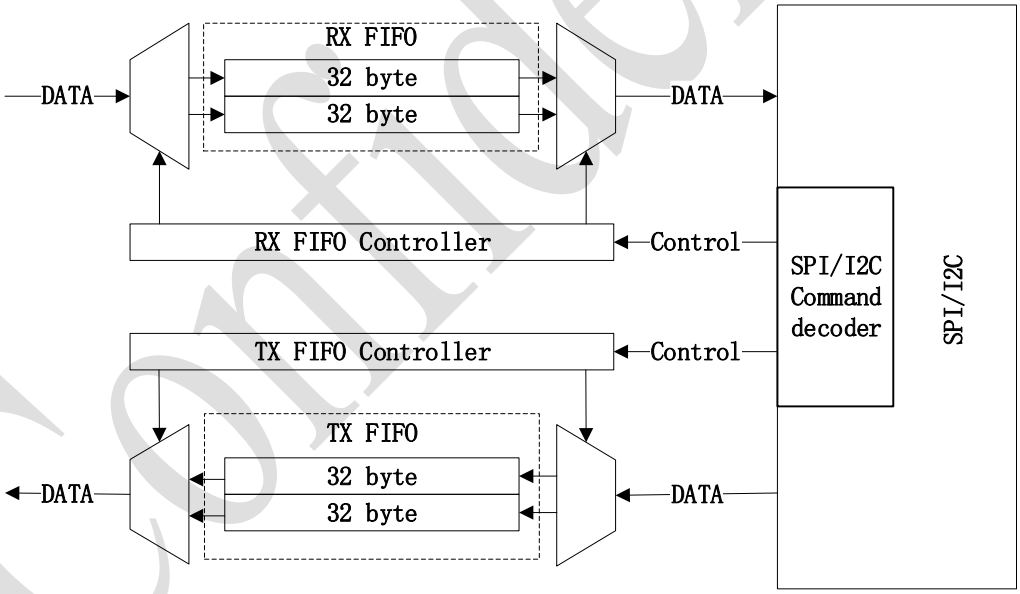


Figure 6-4 Data FIFO Diagram

PAN1026 contains TX_FIFO and RX_FIFO. FIFO can be read and written by SPI commands. In TX mode, TX_FIFO is written by W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK instructions. If a MAX_RT interrupt is generated, the data in TX_FIFO will not be cleared. In the RX mode, the payload in RX_FIFO is read by R_RX_PAYLOAD instruction and the length of the payload is read by the R_RX_PL_WID instruction. The FIFO_STATUS register indicates the status of the FIFO.

6.9 Interrupt Pin

The interrupt pin (IRQ) of the PAN1026 is triggered by a low level and the initial state of the IRQ pin is set high. When TX_DS, RX_DR or MAX_RT in the status register is 1 and the corresponding interrupt report enable bit is 0, interrupt of IRQ pin will be triggered. If MCU writes '1' to the corresponding interrupt source, the interrupt will be cleared. The interrupt trigger of the IRQ pin can be shielded or enabled by setting the interrupt report enable bit to 1 to prohibit the interrupt trigger of the IRQ pin.

7 Data Packet Format

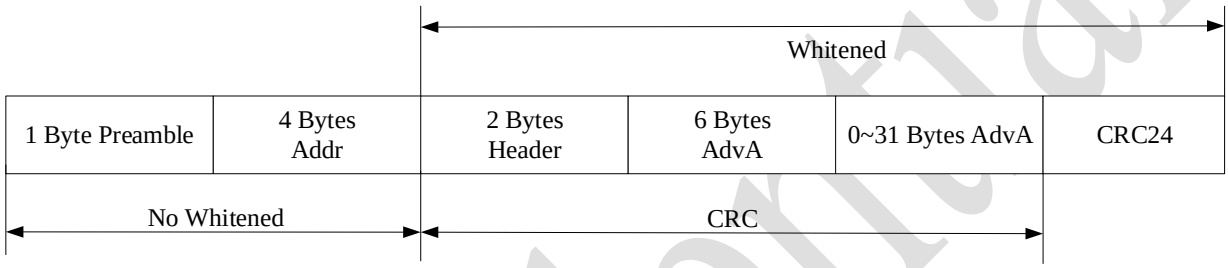
7.1 BLE packet format

The BLE packet format is shown in Table 7-1.

The 6th and 7th bytes of AdvD can be used as filter bytes. Use register WL_MATCH_MODE to select 0~2 Bytes for matching.

Note: 2-byte header is stored in FIFO.

Table 7-1 BLE Packet Format



7.2 Data Packet Format Compatible with XN297L

7.2.1 Data Packet Format in Normal Mode

The data packet format of normal mode is shown in Table 7-2, Naming frame mode I.

The address and data part in Table 7-2 can choose the scrambling code mode, according to the enable/disable scrambling code configuration bit.

Table 7-2 Data Packet Format in Normal Mode

Preamble (3 bytes)	Address (3~5 bytes)	Data (1~32/64 bytes)	CRC (1/2 bytes)

7.2.2 Data Packet Format in Enhanced Mode

The data packet format of the enhanced mode is shown in Table 7-3, Naming frame mode II.

In Table 7-3, the scrambling code mode can be selected by the address, CRC and data part according to the enable/disable scrambling code configuration bit.

Table 7-3 Data Packet Format in Enhanced Mode

Preamble (3 bytes)	Address (3~5 bytes)	Identification (10bits)			Data (1~32/64 bytes)	CRC (1/2 bytes)
		Data length (7bits)	PID (2bits)	NO_ACK (1bit)		

7.2.3 ACK Packet Format in Enhanced Mode

The ACK packet format of the enhanced mode is shown in Table 7-4, Naming frame mode III.

The address and CRC part in Table 7-4 need to be selected the same as PTX.

Table 7-4 Enhanced Mode ACK Packet Format

Preamble (3 bytes)	Address (3~5 bytes)	Identification (10bits)			CRC (1/2 bytes)
		Data length (7bits)	PID (2bits)	NO_ACK (1bit)	

8 SPI/I2C Control Interface

The MCU can read and write the registers of PAN1026 by the SPI/I2C control interface. As a slave, the data rate of SPI/I2C interface depends on the speed of MCU. The highest speed of four-wire SPI is 16Mbps. The highest speed of three-wire SPI is 2Mbps(Current test results).The highest speed of I2C is 1.5Mbps.

The SPI interface is shown in Table 8-1. The general I/O port of the MCU can be used to simulate the timing of standard SPI . When the CSN pin is 0, the SPI interface waits for the command to be executed. One instruction will be executed once the CSN pin changes from 1 to 0. After the CSN pin changes from 1 to 0, the contents of the status register can be read by MISO.

Table 8-1 Four-wire SPI Interface

Pin name	I/O	SPI function description
CSN	I	Chip select enable signal, active at low level
SCK	I	Clock
MOSI	I	Serial input
MISO	O	Serial output

Table 8-2 Three-wire SPI Interface

Pin name	I/O	SPI function description
CSN	I	Chip select enable signal, active at low level
SCK	I	Clock
MOSI	I/O	Data input and output interface
MISO	High resistance	Reserved

The I2C interface is shown in Table 8-3. It is used to read and write internal registers and FIFOs. Among them, SCL is multiplexed with SCK of SPI interface. SDA is multiplexed with MOSI of SPI interface. CSN must always be high in I2C mode. The I2C pad was internally pulled up with a resistance of 4.7K. The pull-up function of I2C pads can be disabled by controlling the registers of CSK_PAD_PU and MOSI_PAD_PU. Normally, the pull-up function is enabled by default.

Since the I2C protocol circuit of the 3V register is shared with the 1.8V register, there is only one I2C device communication address(0x71).

Table 8-3 I2C Interface

Pin name	I/O	I2C function description
CSN	I	High level
SCL	I	Multiplexing with SCK
SDA	I/O	Multiplexing with MOSI
MISO	High resistance	Reserved

8.1 SPI Command Format

<Command word: from high bits to low bits (per byte)>

<Data byte: from low bytes to high bytes. Bits in each byte are from high to low.>

Table 8-4 SPI Command Format

Command name	Command word	Command word (Binary)	With data (Number of bytes)	Operation
W_PAGE_OF_1P8V_REG	0xF0	1111 0000	1	Write the page of the 1.8V register, most are located on page0, and some are located on page1
R_PAGE_OF_1P8V_REG	0xFE	1111 1110	1	Read the page of the 1.8V register, most are located on page0, and some are located on page1
R_REGISTER	0x00+addr	000A AAAA	1 to 5 low byte first	Read status register AAAAA=5bit register address
W_REGISTER	0x20+addr	001A AAAA	1 to 5 low byte first	Write status register AAAAA=5bit register address Only be executed in DEEP_SLEEP and standby mode-I.
R_RX_PAYLOAD	0x61	0110 0001	1 to 32/64 low byte first	Read the received data, the read operation usually starts from the byte 0. After finishing reading, the data will be deleted from the RX FIFO. The operation will be executed in the receive mode.
W_TX_PAYLOAD	0xA0	1010 0000	1 to 32/64 low byte first	Write transmitting data, the write operation usually starts from byte 0.
FLUSH_TX	0xE1	1110 0001	0	Clear TX FIFO, executed in TX mode.
FLUSH_RX	0xE2	1110 0010	0	Clear RX FIFO, executed in RX mode.
REUSE_TX_PL	0xE3	1110 0011	0	Used on the PTX side, the data sent in the last frame is used again and sent. This command is available after data transmission or execution of FLUSH_TX command. This command cannot be used in the process of data transmission.
ACTIVATE	0x50	0101 0000	1	With this command followed by data 0x73, the following functions will be activated. • R_RX_PL_WID • W_TX_PAYLOAD_NOACK The function above will be turned off if the same data follows this command again. This command is only executed in DEEP_SLEEP mode and standby mode-I.
DEACTIVATE	0x50	0101 0000	1	With this command followed by data 0x8C, the following functions will be turned off. • R_RX_PL_WID • W_TX_PAYLOAD_NOACK • W_ACK_PAYLOAD
R_RX_PL_WID	0x60	0110 0000	0	Read the RX-payload data width at the top of the

				RX FIFO.
W_ACK_PAYLOAD	0xA8+ PPP	1010 1PPP	1 to 32/64 low byte first	Executed in RX mode Write PIPE PPP (the value of PPP is from 000 to 101) when responding to ACK and return data. Up to 2 ACK packets can be set. Data from the same PIPE will be sent based on first-in, first-out. Write operations usually start from byte 0.
W_TX_PAY-LOAD_NOACK	0xB0	1011 0000	1 to 32/64 low byte first	Write transmitted data, the write operation usually starts from byte 0. When executed in TX mode, this command is used to send data. After sending, the TX_DS flag will be set and won't be any automatic response.
3V_REG0_WR	0xF1	1111 0001		Write 3V_register_0
3V_REG0_RD	0xF2	1111 0010		Read 3V_register_0
3V_REG1_WR	0xF3	1111 0011		Write 3V_register_1
3V_REG1_RD	0xF4	1111 0100		Read 3V_ register_1
CE_SPI_ON	0xFD	1111 1101	00	Set CE internal logic to 1
CE_SPI_OFF	0xFC	1111 1100	00	Set CE internal logic to 0
RST_SPI_HOLD	0x53	0101 0011	1	Use this command followed by the data 0x5A to enter the reset state and keep it.
RST_SPI_RELS	0x53	0101 0011	1	Use this command followed by data 0xA5 to release the reset state and operate normally.
NOP	0xFF	1111 1111	0	No operation

R_REGISTER and W_REGISTER registers may operate single-byte or multi-byte registers. When accessing a multi-byte register, the highest bit of the lowest byte should be read/written first. Only part bytes of the multi-byte register can be modified. The higher bytes that are not written keep the original content. For example: the lowest byte of the RX_ADDR_P0 register can be changed by writing a byte of the register RX_ADDR_P0.

8.2 3-wire SPI Timing

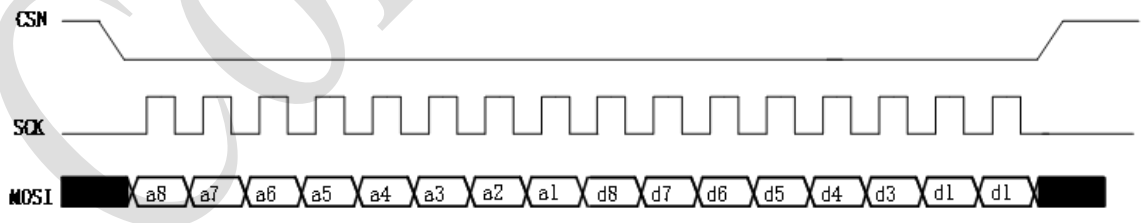


Figure 8-1 3-wire SPI Timing

Reading and writing of 3-wire SPI share the same time sequence. The difference is that data is input when writing and data is output when reading.

8.3 I2C Timing

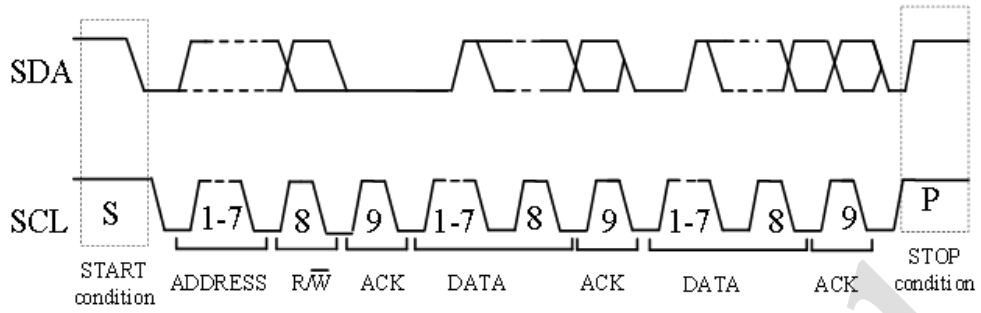


Figure 8-2 I2C Timing

8.4 4-wire SPI timing

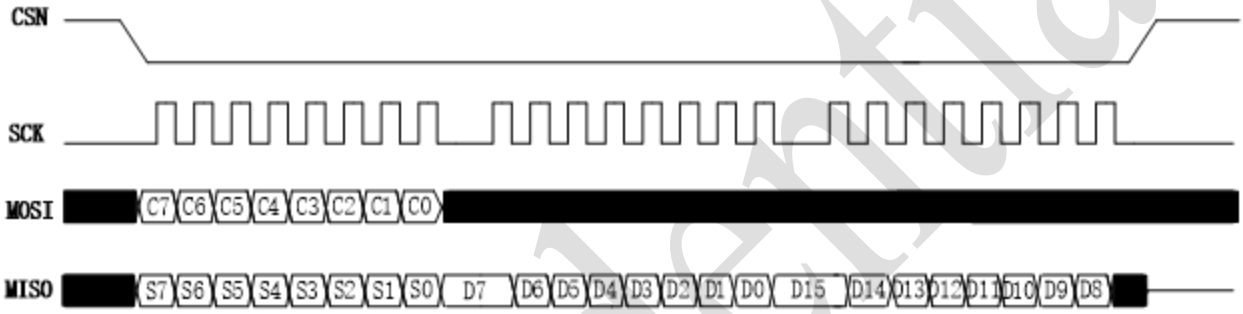


Figure 8-3 3-wire SPI Reading Operation

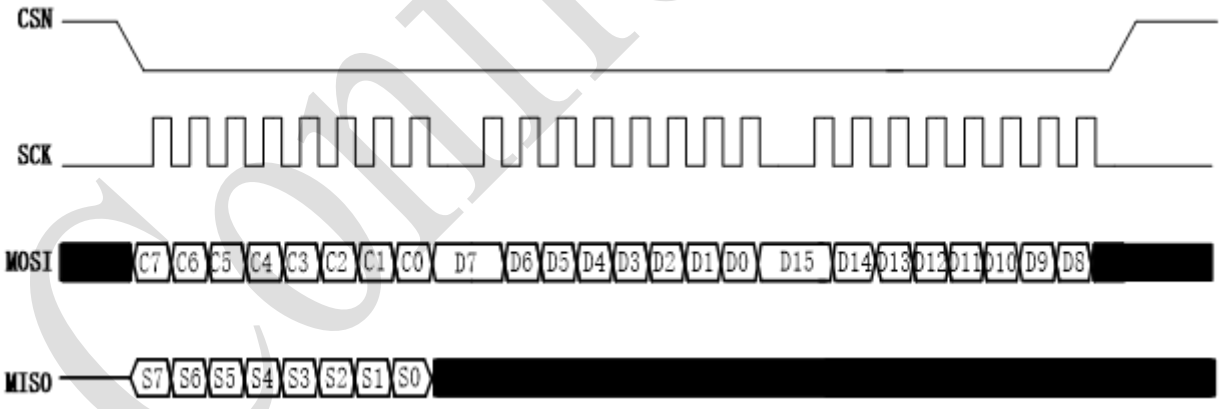


Figure 8-4 3-wire SPI Writing Operation

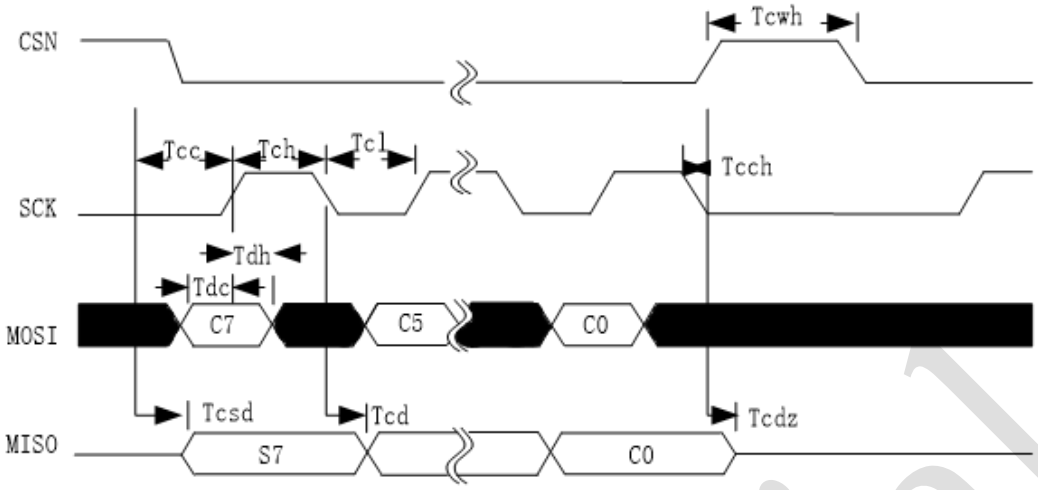


Figure 8-5 SPI, NOP Operation Timing Diagram

Table 8-5 SPI Operation Reference Time

Symbol	Parameters	Min	Max	Units
Tdc	Set up time of data	15	-	ns
Tdh	Hold time of data	2	-	ns
Tcl	Time that SCK is at low level	31.25	-	ns
Tch	Time that SCK is at high level	31.25	-	ns
Fsck	Frequency of SCK	-	16	MHz
Tcc	Set up time of CSN	2	-	ns
Tcch	Hold time of CSN	2	-	ns
Tcwh	Invalid time of CSN	49	-	ns
Tcdz	Time that CSN is high impedance	-	40	ns

*Note: The parameters in Table 8-5 can be adjusted according to the selected MCU.

Figure 8-3~Figure 8-5 and Table 8-5 show the SPI operation and timing sequence. The following symbols are used in the figure:

-SPI instruction bit

-Status register bit

-Data bit (note: from low byte to high byte, high bit in front in each byte)

among them: i=1, 2, 3, …n

9 Control Register

The registers in the table can be reads and writes to configure and control PAN1026 through SPI/I2C. The result of the registers that are not defined in the table is 0.

9.1 Register Map

CMD (hex)	Register	BIT	Defaults	W/R	Description
F1 write F2 read	3V_REG0_WR	7: 0	0x14	W/R	3V register
	Reserved	7: 5	000		Reserved
	CSK_PAD_PU	4	1		Pull up control bit of CSK PAD. In 4-wire SPI mode, this bit should set to 0. In 3-wire SPI mode, this bit is automatically switched to 0. In I2C mode, this bit should be set to 1. 0: Turn off pull-up. 1: Open pull-up.
	CSK_PAD_PD	3	0		Pull-down control bit of CSK PAD. 0: Turn off pull-down. 1: Open drop-down
	CSN_PAD_PU	2	1		Pull-up control bit of CSN PAD. The pull-up resistor is 234K: 0: Turn off pull-up. 1: Open pull-up.
	CSN_PAD_PD	1	0		Pull-down control bit of CSN PAD. 0: Turn off pull-down. 1: Open drop-down.
	NRESET_1P8V	0	0		1.8V logic reset control bit. 0: 1.8V logic resets. 1: 1.8V logic works normally.
F3 写 F4 读	3V_REG1_WR	15: 0	0x0D40		3V register
	EN_COUNTER	15	0		Enable bit of the fast startup clock's counter buffer. 1: Enabled. 0: Disabled.
	COUNT_EXTEND	14	0		3V control signal of the fast startup XTAL oscillator. This bit selects the number of the counter bits (the duration of delay). 1: (2^11)/16M 0: (2^10)/16M
	EN_CONT_RST	13	0		The 3V reset signal of the counter in the fast startup XTAL oscillator.

					0: Reset. 1: Release reset.
	EN_STARTUP	12	0		The 3V control signal of the fast startup XTAL oscillator. Enable bit of the fast startup circuit. 1: Enabled. 0: Disabled.
	MOSI_PAD_DIEN	11	1		PAD MOSI working mode selection bit. 0: Digital output/analog mode. 1: Digital input mode.
	MOSI_PAD_PU	10	1		Pull-up control bit of MOSI PAD. In 4-wire SPI mode, this bit should be set to 0. In 3-wire SPI mode, this bit is automatically switched to 0. In I2C mode, this bit is set to 1. 0: Turn off pull-up. 1: Open pull-up.
	MOSI_PAD_PD	9	0		Pull-down bit of MOSI PAD output. 1: Pull down. 0: Not pull down.
	SPI_3_WIRE_EN	8	1		Enable bit of 3-wire SPI. 0: 4-wire SPI 1: 3-wire SPI (MISO_PAD will not be used.)
	MISO_PAD_DIEN	7	0		Mode selection of PAD MISO. 0: Digital output/analog mode. 1: Digital input mode.
	MISO_PAD_OE	6	1		Enable bit of MISO PAD output. 1: Output mode. 0: Input mode.
	MISO_PAD_PU	5	0		Pull-up control bit MISO PAD output. 1: Pull up. 0: Not pull up.
	MISO_PAD_PD	4	0		Pull-down control bit of MISO PAD output. 1: Pull down. 0: Not pull down.
	PWR_UP	3	0		The 3V control signal to enable the XTAL oscillator. 1: Enabled. 0: Disabled.
	EN_LS	2	0		The 3V control signal of level shift. 1: Enabled. 0: Disabled.
	EN_LDO_DVDD	1	0		The 3V control signal to enable the 1.8V digital LDO DVDD. 1: Enabled.

					0: Disabled.
	EN_PM	0	0		The 3V control signal to enable the PMU, including bandgap, current, etc. 1: Enabled. 0: Disabled.

9.2 1.8V Register Map

9.2.1 PAGE0

Address (hex)	Register	BIT	Defaults	W/R	Description
00	CONFIG	7: 0	0x06		Working configuration register
	WORK_MODE	7: 6	00	R/W	Working mode selection: 00: 297L mode. 01: BLE broadcast packet mode. 10: Reserved. 11: Reserved.
	MASK_RX_DR	5	0	R/W	The interrupt report enable bit for successful data reception: 1: The interrupt is not reflected to the IRQ pin. 0: RX_DR interrupt is reflected to IRQ pin.
	MASK_TX_DS	4	0	R/W	The interrupt report enable bit for successful data transmission: 1: The interrupt is not reflected to the IRQ pin. 0: TX_DS interrupt is reflected to IRQ pin.
	MASK_MAX_RT	3	0	R/W	The interrupt report enable bit when the number of transmission failure reaches the maximum: 1: The interrupt is not reflected to the IRQ pin. 0: MAX_RT interrupt is reflected to IRQ pin.
	CRC16_SEL	2	1	R/W	1: CRC16 0: CRC8
	CRC_EN	1	1	R/W	CRC enable bit: 1: CRC is enabled. 0: CRC is disabled.
	PRIM_RX	0	0	R/W	RX/TX control bit: 1: PRX. 0: PTX.
01	EN_AA	7: 0	0x01		Automatic answer enable bit of receiving channel.
	RF_DR[1: 0]	7: 6	00	R/W	Analog filter rate setting bits. The configure of DIG_DR in MDM should be separate with these bits. 01: 2Mbps.

					00: 1Mbps. 11: 250kbps
	ENAA_P5	5	0	R/W	Enable pipe5 auto answer.
	ENAA_P4	4	0	R/W	Enable pipe4 auto answer.
	ENAA_P3	3	0	R/W	Enable pipe3 auto answer.
	ENAA_P2	2	0	R/W	Enable pipe2 auto answer.
	ENAA_P1	1	0	R/W	Enable pipe1 auto answer.
	ENAA_P0	0	1	R/W	Enable pipe0 auto answer.
02	AW_RXADDR	7: 0	0xC1		Receive channel enable bit.
	AW	7: 6	11	R/W	RX/TX address width. If the address width set is lower than 5 bytes, the lower bits will be used: 00: invalid. 01: 3 bytes. 10: 4 bytes. 11: 5 bytes.
	ERX_P5	5	0	R/W	Enable data pipe 5.
	ERX_P4	4	0	R/W	Enable data pipe 4.
	ERX_P3	3	0	R/W	Enable data pipe 3.
	ERX_P2	2	0	R/W	Enable data pipe 2.
	ERX_P1	1	0	R/W	Enable data pipe 1.
	ERX_P0	0	1	R/W	Enable data pipe 0.
03	SETUP_RX	23: 0	0x5D501E		Receive channel settings.
	BN_CTM[2: 0]	23: 21	010	R/W	Tuning capacitor control bit for balun's low noise amplifier interface.
	LNA_GC[1: 0]	20: 19	11	R/W	LNA gain control bit. 11: High gain. 00: Low gain.
	LNA_BC	18	1	R/W	LNA current control bit. 1: High current. 0: Low current.
	LNA_CTM[2: 0]	17: 15	010	R/W	LNA and PA drive load capacitance control.
	BPF_CTRL_GAIN	14	1	R/W	BPF gain control bit. 0: High gain. 1: Low gain.
	BPF_CTRL_BW	13	0	R/W	BW control additional bit.
	IB_BPF_TRIM	12	1	R/W	Control BPF current.
	Reserved	11: 8	0000	-	-
	BW_500K	7	0	R/W	500K bandwidth (same as XN297L).
	GC_500K	6	0	R/W	500K gain control.
	RCCAL_IN[5: 0]	5: 0	011110	R/W	Manual control of RC calibration signal.
04	SETUP_RETR	7: 0	0x03		Automatic transfer settings.
	ARD	7: 4	0000	R/W	Automatic transmission delay:

					0000: 250μs 0001: 500μs 0010: 750μs ... 1111: 4000μs
	ARC	3: 0	0011	R/W	Setting for the times of automatic transmission: 0000: Communication mode without automatic re-transmission and ACK. 0001～1111: Communication mode with automatic retransmission. 0001: 1 transmission with ACK. 0010: 2 transmissions with automatic retransmission and ACK. ... 1111: 15 transmissions with automatic retransmission and ACK.
05	RF_CH	15: 0	0x008E	-	Communication channel settings.
	Reserved	15: 9	0000000	-	-
	HIGH_RF	8	0	R/W	Frequency selection of RX: 0: High frequency, channel + 2M. 1: Low frequency, channel-2M.
	RF_CH	7: 0	10001110	R/W	Channel=RF_CH + 2336 Set the channel used by TX: Channel=RF_CH + 2336
06	SETUP_RXTX	23: 0	0x492A48		Communication parameter configuration.
	AMP_SEL_I[2: 0]	23: 21	010	R/W	Non-inverting LO buffer amplitude control.
	AMP_SEL_Q[2: 0]	20: 18	010	R/W	Quadrature LO buffer amplitude control.
	PH_SEL_I[2: 0]	17: 15	010	R/W	In-phase LO buffer phase control.
	PH_SEL_Q[2: 0]	14: 12	010	R/W	Quadrature LO buffer phase control.
	RCCAL_EN	11	1	R/W	The enable signal of the calibration in the receiving bandpass filter: 1: Enabled. 0: Disabled.
	Reserved	10	0	-	-
	DA_GC	9	1	R/W	DAC gain control bit. 1: High gain. 0: Low gain.
	DA_LPF_BW	8	0	R/W	BW control 1Mbps or 2Mbps DAC output filter.
	DA_VREF_MB[2: 0]	7: 5	010	R/W	DAC high reference voltage control.
	DA_VREF_LB[2: 0]	4: 2	010	R/W	DAC low reference voltage control.
	DIG_DR[1: 0]	1: 0	00	R/W	MDM rate setting. The configuration of this bit should be separate with analog filter: 01: 2Mbps

					00: 1Mbps 11: 250kbps
07	STATUS	7: 0	0x0E	-	Status register
	Reserved	7	0	-	-
	RX_DR	6	0	R/W	The control signal of the received data interrupt in RX FIFO. Interrupt is generated when new data is in RX FIFO. Write 1 to clear interrupt.
	TX_DS	5	0	R/W	The interrupt control bit when TX FIFO successfully transmits data. In the mode without automatic retransmission, interrupt is generated after the successful data transmission. In the mode with automatic retransmission, only when the transmitter receives ACK, this bit will be set high. Write 1 to clear interrupt.
	MAX_RT	4	0	R/W	The interrupt control bit when the number of transmission reaches the maximum. Write 1 to clear interrupt. After the interrupt is generated, the interrupt must be cleared to continue communication.
	RX_P_NO	3: 1	111	R	The pipe number that can be read from RX_FIFO: 000-101: Pipe number. 110: Not Used. 111: Empty RX_FIFO.
	TX_FULL	0	0	R	The flag that shows whether TX FIFO is full: 1: TX FIFO is full. 0: TX FIFO is not full and available.
08	OBSERVE_TX	7: 0	0x00	-	Transfer status register.
	PLOS_CNT	7: 4	0000	R	Packet loss counter. The counter will stop counting when it reaches the maximum value of 15. The counter is reset when RF_CH is written. Communication continues when the value is not reset.
	ARC_CNT	3: 0	0000	R	Transmission counter for automatic retransmission. Once automatic retransmission happens, the value in ARC_CNT increases by one. When ARC_CNT reaches the ARC limit value, it will be regarded as a packet loss and PLOS_CNT will increase by one. The counter will be reset when new data is written into the TX FIFO.
09	DATAOUT	15: 0	0x8000		Read-only register.
	VCO_CODE_VAL[3: 0]	15: 12	1000	RO	VCO correction result.

	Reserved	11: 7	00000	-	-
	CHIRPFLAG	6	0	RO	The read-only signal of the fast startup XTAL oscillator: 1: Fast startup circuit is working. 0: Fast startup circuit is not working.
	RCCAL_VAL[5: 0]	5: 0	000000	RO	-
0A	RX_ADDR_P0	39: 0	0xE7E7E7E7E7	R/W	The receiving address of data pipe 0, up to 5 bytes. (Write from the lower bits. The length of address is defined by AW.)
0B	RX_ADDR_P1	39: 0	0xC2C2C2C2C2	R/W	The receiving address of data pipe 1, up to 5 bytes. (Write from the lower bits. The length of address is defined by AW.)
0C	RX_ADDR_P2P3	15: 0	0xC3C4	-	-
	RX_ADDR_P2	15: 8	0xC3	R/W	The receiving address of data pipe 2. It is only the lowest 8 bits. The higher bits are to the same as RX_ADDR_P1[39:8]
	RX_ADDR_P3	7: 0	0xC4	R/W	The receiving address of data pipe 3. It is only the lowest 8 bits. The higher bits are to the same as RX_ADDR_P1[39:8].
0D	RX_ADDR_P4P5	15: 0	0xC5C6	-	-
	RX_ADDR_P4	15: 8	0xC5	R/W	The receiving address of data pipe 4. It is only the lowest 8 bits. The higher bits are to the same as RX_ADDR_P1[39: 8]
	RX_ADDR_P5	7: 0	0xC6	R/W	The receiving address of data pipe 5. It is only the lowest 8 bits. The higher bits are to the same as RX_ADDR_P1[39: 8]
0E	SETUP_RF	15: 0	0x3FFB	-	-
	TXSYN_ALWAYS_ON	15	0	R/W	1: EN_TX_SYN is always high. 0: EN_TX_SYN is controlled by the state machine
	RXSYN_ALWAYS_ON	14	0	R/W	1: EN_RX_SYN is always high. 0: EN_RX_SYN is controlled by the state machine
	EN_RX_LNA	13	1	R/W	Receive LNA enable control bit. 1: Enabled 0: Disabled
	EN_RX_MIX	12	1	R/W	Receive mixer enable control bit. 1: Enabled 0: Disabled
	EN_RX_BPF	11	1	R/W	Receive filter enable control bit. 1: Enabled 0: Disabled
	EN_RX_LIMITER	10	1	R/W	Receive LIMITER enable control bit. 1: Enabled 0: Disabled

	EN_RX_DPLL	9	1	R/W	Receive DPLL enable control bit. 1: Enabled 0: Disabled
	EN_TX_DAC	8	1	R/W	Transmit DAC enable control bit. 1: Enabled 0: Disabled
	EN_TX_PABUF	7	1	R/W	Transmit PA buf enable control bit. 1: Enabled 0: Disabled
	EN_SYN_PFD	6	1	R/W	PLL PFD enable control bit. 1: Enabled 0: Disabled
	EN_SYN_CP	5	1	R/W	PLLCP enable control bit. 1: Enabled 0: Disabled
	CAL_VREF_SEL	4	1	R/W	VCO Calibration reference voltage control.
	EN_XTAL_FB	3	1	R/W	Crystal oscillator feedback loop control bit. 1: Closed loop 0: Open loop
	XTAL_FC[2: 0]	2: 0	011	R/W	Fine tuning control of crystal frequency.
0F	AGC_TABLE[47: 0]	47: 0	0xfffff79c4100	R/W	AGC gain control look-up table.
10	TX_ADDR	39: 0	0xE7E7E7E7E7	R/W	Transmitter address (write from the lower byte) It can only be used in a chip configured in PTX mode. It is necessary to set RX_ADDR_P0 equal to this address to receive an ACK automatic response.
11	RX_PW_P0	7: 0	0x00	-	Data length of RX payload in data pipe 0.
	Reserved	7	0	-	-
	RX_PW_P0	6: 0	0000000	R/W	The data length of the RX payload in data pipe 0. (1 to 32/64 bytes) 0 = The Pipe is not used. 1 = 1 byte. … 32/64 = 32/64bytes.
12	RX_PW_P1	7: 0	0x80	-	Data length of RX payload in data pipe 1.
	IBUF2X	7	1	R/W	LO buf I current control bit: 0: Minimum current. 1: Double the current.
	RX_PW_P1	6: 0	0000000	R/W	The data length of the RX payload in data pipe 1. (1 to 32/64 bytes) 0 = The Pipe is not used. 1 = 1 byte. …

					32/64 = 32/64bytes.
13	RX_PW_P2	7: 0	0x80	-	Data length of RX payload in data pipe 2.
	IRQ_OE	7	1	R/W	IRQ PAD multiplexing bit. 0: Test function PAD. 1: IRQ function PAD.
	RX_PW_P2	6: 0	0000000	R/W	The data length of the RX payload in data pipe 2. (1 to 32/64 bytes) 0 = The Pipe is not used. 1 = 1 byte. … 32/64 = 32/64bytes.
14	RX_PW_P3	7: 0	0x00	-	Data length of RX payload in data pipe 3.
	AGC_GAIN_RST	7	0	WO	When AGC is enabled, reset RX GAIN to the maximum value. It is a write-only register and can be automatically cleared after writing 1.
	RX_PW_P3	6: 0	0000000	R/W	The data length of the RX payload in data pipe 3. (1 to 32/64 bytes) 0 = The Pipe is not used. 1 = 1 byte. … 32/64 = 32/64bytes.
15	RX_PW_P4	7: 0	0x00	-	Data length of RX payload in data pipe 4.
	AGC_EN	7	0	R/W	Receive channel AGC enable bit. 1: Enabled. 0: Disabled.
	RX_PW_P4	6: 0	0000000	R/W	The data length of the RX payload in data pipe 4. (1 to 32/64 bytes) 0 = The Pipe is not used. 1 = 1 byte. … 32/64 = 32/64bytes.
16	RX_PW_P5	7: 0	0x00	-	Data length of RX payload in data pipe 5.
	RX_DATA_JUST	7	0	R/W	It will affect the generation of rx_data_mark in FSM. XN297L is always low.
	RX_PW_P5	6: 0	0000000	R/W	The data length of the RX payload in data pipe 5. (1 to 32/64 bytes) 0 = The Pipe is not used. 1 = 1 byte. … 32/64 = 32/64bytes.
17	FIFO_STATUS	7: 0	0x11	RO	FIFO status register
	CLOCK_RDY	7	0	R	The read-only signal for fast startup XTAL. Delayed by 3 clock cycles than COUNT_DONE.

	TX_REUSE	6	0	R	Call the indicator bit sent by the previous frame of data. After using the REUSE_TX_PL command, this bit will be set to 1 and the last frame of data in the previous transmission will be retransmitted. This bit can be reset by commands W_TX_PAYLOAD, W_TX_PAYLOAD_NOACK, DEACTIVATE, FLUSH TX.
	TX_FULL	5	0	R	TX FIFO full flag. 1: TX FIFO is full. 0: TX FIFO is available.
	TX_EMPTY	4	1	R	TX FIFO empty flag. 1: TX FIFO is empty. 0: TX FIFO is available.
	VCO-CAL_1TIME_FLAG	3	0	R	The flag that shows VCO is calibrated once. It is valid when EN_VCOCAL_ONLY1 is set to 1: 1: VCO has been calibrated once. 0: No VCO calibration has been done
	Reserved	2	0	-	-
	RX_FULL	1	0	R	RX FIFO full flag. 1: RX FIFO is full. 0: RX FIFO is available.
	RX_EMPTY	0	1	R	RX FIFO empty flag. 1: RX FIFO is empty. 0: RX FIFO is available.
18	SETUP_PLL	23: 0	0x4460AC	-	PLL related register settings.
	RX_VCO_BIAS[3: 0]	23: 20	0100	R/W	RX VCO current control.
	TX_VCO_BIAS[3: 0]	19: 16	0100	R/W	TX VCO current control.
	VCO_CT[1: 0]	15: 14	01	R/W	VCO manual capacitor controller.
	PRE_BC[2: 0]	13: 11	100	R/W	Prescaler bias current control.
	BUF_IC[1: 0]	10: 9	00	R/W	LO buffer current control.
	CPSEL[1: 0]	8: 7	01	R/W	Charge pump current control.
	IVCO_SEL[1: 0]	6: 5	01	R/W	VCO-PTAT and bandgap current selection.
	OSC_IC	4	0	R/W	Oscillator current control bit.
	PRE_EN	3	1	R/W	Prescaler enable bit.
	DIV2_IB[2: 0]	2: 0	100	R/W	VCO divider current control bit.
19	DEMOD_CAL	7: 0	0x0F	-	Modulation and demodulation parameter register. (configurable according to the needs of the project)
	CHIP	7	0	R/W	Set whether the chip enters the test mode: 1: Enter test mode. 0: Exit test mode.
	CARR_MOSI	6	0	R/W	Substitute MOSI with single carrier. it only affects RX.

					1: CHIP=1 & CE=1 & en_rx_mode=0, EN_RF_RX=1 0: CHIP=1 & CE=1 & en_rx_mode=0, EN_RF_RX=0
	CARR_CSK	5	0	R/W	Substitute CSK with single carrier. It affects both TX and RX. Impact on TX: 1: CHIP=1 and CE=0, EN_RF_TX=1 0: CHIP=1 and CE=0, EN_RF_TX=0 Impact on RX: 1: CHIP=1 and CE=1 and en_rx_mode=1, EN_RF_RX=1 0: CHIP=1 and CE=1 and en_rx_mode=1, EN_RF_RX=0
	GAUS_CAL	4: 1	0111	R/W	Control signal to adjust the amplitude of the signal from Gaussian filter to DAC. The amplitude of the output signal is one of the determinants of the frequency deviation in the transmit modulation: 1111: Low signal. … 1000: Medium signal. … 0000: Large signal.
	SCR_EN	0	1	R/W	Scrambling function enable bit: 1: Enable. 0: Disabled.
1A	RF_CAL2	23: 0	0xDFCC00	-	Additional RF register. (usually use the default value)
	LOBUF_EN	23	1	R/W	LO buffer enable signal.
	QBUF2X	22	1	R/W	LO buf Q channel current control bit: 0: The minimum current is equal to the I current. 1: Q channel current is doubled.
	FREQ_SEL	21	0	R/W	Switch of small KVCO's variable capacitor in transceiver: 1: RX mode. 0: TX mode.
	PA_GC[2: 0]	20: 18	111	R/W	PA output power control.
	RF_PA_PWR[2: 0]	17: 15	111	R/W	PA output power (tentative) control
	PA_RAMP_SEL[1: 0]	14: 13	10	R/W	PA ramp selection method: 00: NO ramp 01: 1 us ramp UP & DOWN each step. 10: 2 us ramp UP & DOWN each step. 11: 4 us ramp UP & DOWN each step.

	PMU_IBG_RES[1: 0]	12: 11	01	R/W	The control bit of resistor to control the current of Bandgap.
	PMU_VBG_TRIM[4: 0]	10: 6	10000	R/W	Bandgap voltage trimming controller.
	LDO_VSEL_1P8	5	0	R/W	1.8V LDO voltage controller.
	Reserved	4	0	-	-
	TST_BPF	3	0	R/W	Test BPF filter output.
	TST_DAC	2	0	R/W	Test DAC voltage.
	TST_MIXER	1	0	R/W	Test MIXER output.
	TST_VC	0	0	R/W	Test PLL control voltage.
1B	DEM_CAL2	23: 0	0x00DF0B	-	Additional demodulation parameter register. (usually use the default value)
	PIN	23: 21	000	R/W	Set the output PIN (MISO pin/IRQ pin) after the chip enters the test mode: 000 (and CHIP is 0) is the working mode for data output and interrupt output. 000 (and CHIP is 1) is the sensitivity test mode for demodulation data and clock output. 110 (and CHIP is 1) is the receiving test mode, with two outputs of limit I and Q.
	EN_RX	20	0	R/W	Whether the receiving channel and the phase-locked loop are turned on at the same time: 1: Open at the same time. 0: Open at different time.
	DELAY1	19	0	R/W	The signal shows whether the PLL is open-loop. The open-loop PLL can be used to test the transmission carrier drift. 1: PLL is open loop. 0: PLL open loop is controlled by state machine
	DELAY0	18	0	R/W	Whether the demodulator superimposes the initial offset of the reception. When the demodulator does not superimpose the initial offset, test of receiving sensitivity can be done. 1: Do not superimpose the initial offset. 0: The initial frequency offset is superimposed and the bit error caused by the center frequency offset can be offset in the receiving state
	TH1	17	0	R/W	In transmit single carrier test mode, whether LDO (except DVDD LDO) is enabled: 1: EN_LDO_1P8V=1 0: EN_LDO_1P8V=ldo_en (state machine control)
	PTH	16: 13	0110	R/W	Preamble correlation threshold setting of receiver digital demodulator, correlation threshold of 24-bit

					preamble=PTH+16: 1000: 24 bits 0110: 22 bits 0000: 16 bits
	SYNC_SEL	12	1	R/W	4 times the sampling of the receiver's digital demodulator, take a few points to calculate the correct data: 1: 3bit 0: 2bit
	DECOD_INV	11	1	R/W	Whether the preamble is inverted by bit. Generally, this bit is set to 1. Both receiver and transmitter should enable this function: 1: No inversion bit. 0: Invert by bit.
	GAIN1	10: 7	1110	R/W	Frequency loop gain1, set to 1110.
	GAIN2	6: 1	000101	R/W	Frequency loop gain2, set to 000101
	AGGRESSIVE	0	1	R/W	Speed selection of the rate synchronization unit of the demodulator: 1: Large step size adjustment, fast speed. 0: Small step size adjustment, slow speed.
1C	DYNPD		0x00		Dynamic PAYLOAD length enable.
	EN_VCO-CAL_ONLY1	7	0	R/W	The enable signal to ensure the VCO only calibrates once, provided that the frequency point is not switched: 1: Only do VCO calibration once, then TX/RX will not do VCO calibration any more to save the time of calibration. 0: The function is off
	noIRQ_noWORK	6	0	R/W	1: FSM does not work, if IRQ is not cleared. 0: FSM works, even if the IRQ is not cleared.
	DPL_P5	5	0	R/W	Enable of PIPE 5's dynamic PAYLOAD length. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable of PIPE 4's dynamic PAYLOAD length. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable of PIPE 3's dynamic PAYLOAD length. (Requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable of PIPE 2's dynamic PAYLOAD length. (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable of PIPE 1's dynamic PAYLOAD length. (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable of PIPE 0's dynamic PAYLOAD length. (Requires EN_DPL and ENAA_P0)
1D	FEATURE	7: 0	0x00	R/W	Feature register

	IRQ_INV_SEL	7	0	R/W	Whether the IRQ output is inverted: 0: Not inverted. 1: Inverted.
	MUX_PA_IRQ	6	0	R/W	Select IRQ signal output or EN_PA signal to PIN: 0: Output IRQ signal to PIN. 1: Output EN_PA signal to PIN.
	IQ_SW	5	0	R/W	I/Q phase switch.
	DATA_LEN_SEL	4: 3	00	R/W	Data length selection: 11: 64 bytes (512 bit) mode. 00: 32 bytes (256 bit) mode.
	EN_DPL	2	0	R/W	Enable dynamic PAYLOAD length.
	EN_ACK_PAY	1	0	R/W	Enable ACK with PAYLOAD.
	EN_DYN_ACK	0	0	R/W	Enable W_TX_PAYLOAD_NOACK command.
1E	RF_CAL	15: 0	0x0E68		RF parameter register. (configurable according to the needs of the project)
	XTAL_OCLK_OE	15	0	R/W	CLK_OUT PAD multiplexing: 0: Test PAD 1: Clock output PAD
	EN_XTAL_OCLK	14	0	R/W	The enable signal of the buffer in XTAL to output the clock to PAD: 1: Enabled. 0: Disabled.
	CLK_SEL[1: 0]	13: 12	00	R/W	Selection of the frequency from the XTAL oscillator to PAD: 00: 16M 01: 8M 10: 4M 11: 2M
	OTA_GC[2: 0]	11: 9	111	R/W	RX channel gain setting.
	TST_VBG	8	0	R/W	Test bandgap voltage.
	REF_DIV_SEL	7	0	R/W	Reference clock frequency selection: 0: 1M 1: 2M
	VCO_CAL_EN	6	1	R/W	VCO calibration enable.
	VCO_DLY_SEL[1: 0]	5: 4	10	R/W	VCO calibration delay time selection: 00: 3us 01: 6us 10: 9us 11: 12us
	VCO_CODE_IN[3: 0]	3: 0	1000	R/W	VCO code retention.
1F	BB_CAL	39: 0	0x9C600EA50A	-	Digital baseband parameter register. (usually use the default value)

	INVERTER	39	1	R/W	Whether to invert the RX channel data before entering RX_block: 1: Invert. 0: Remain unchanged.
	DAC_MODE	38	0	R/W	dac_out[5:0] whether to invert the output, dac_out[5: 0] is the DAC data input terminal. 1: dac_out[5: 0]<= [0: 5] 0: dac_out[5: 0]<= [5: 0]
	DAC_BASAL	37: 32	011100	R/W	The initial value of the DAC input data in the stage of pre-transmission.
	CE_JUST_TIME	31: 30	01	R/W	The waiting time for the main state machine to enter TX_SET from STANDBY. The length of time is calculated: CE_JUST_TIMEx4, the unit is us, the range is 0~12us, and the default value is 4us.
	LDO_WAIT_TIME	29: 27	100	R/W	LDO stable time, the length of time is calculated: LDO_WAIT_TIME x 8, the unit is us, the range is 0~56us, and the default value is 32us.
	TRX_TIME	26: 23	0000	R/W	The time interval from PLL open loop/PA being enabled (based on the later one) to the start of data transmission. The length of time is calculated: TRX_TIME×8, the unit is us, the range is 0~120us, and the default value is 0us.
	EX_PA_TIME	22: 17	000111	R/W	The time interval from PLL being enabled to PA being enabled. The length of time is caculated: EX_PA_TIME×16, the unit is us, the range is 0~1008us, and the default value is 112us.
	TX_SETUP_TIME	16: 11	010100	R/W	The time interval from when the PLL is enabled to when the PLL opens, and the length of time is calculated: TX_SETUP_TIME×16, the unit is us, the range is 0~1008us, and the default value is 320us.
	RX_SETUP_TIME	10: 6	10100	R/W	The setup time of the PLL in RX. The length of time is calculated: RX_SETUP_TIME×16, the unit is us, the range is 0~496us, the default value is 320us
	RX_ACK_TIME	5: 0	001010	R/W	The longest time to wait for ACK after PTX is switched to receiving mode. The transmission will be considered to be a failure if the interval is longer than the longest waiting time. Time length calculation in 2Mbps mode: RX_ACK_TIME×16, the unit is us. Time length calculation in 1Mbps mode:

					RX_ACK_TIME×32, the unit is us. Time length calculation in 250kbps mode: RX_ACK_TIME×128, the unit is us.

9.2.2 PAGE1

Address (hex)	Register	BIT	Defaults	W/R	Description
00	P1_REG_00	47: 0	0x000000000000	-	-
	WL_ADDR	47: 0	0x000000000000	R/W	Setting of white list address in BLE mode. BLE mode whitelist address configuration. The address is actually a piece of data in the payload, used for RX filtering function. It is recommended to set WL_MATCH_MODE to 1. The 7th byte of the payload can be used as the filter byte. If WL_MATCH_MODE is set as 2, the 6th and 7th bytes of the payload is used as the filter byte.
01	P1_REG_01	7: 0	0x00	-	-
	Reserved	7: 4	0000	R/W	-
	FIR_CUT_MODE	3	0	R/W	fir_filter mode selection in demodulator: 0: 297L mode 1: Added filter overflow protection mode
	WL_MATCH_MODE	2: 0	000	R/W	Whitelist filtering mode selection: 000: Do not filter, report all 001: Just match WL_ADDR[47:40] to report, corresponding to the 7th byte of AdvD 010: Just match WL_ADDR[47:32] to report, corresponding to the 6th and 7th bytes of AdvD 011: undefined 100: undefined 101: undefined 110: undefined 111: Same as 000, report all without filtering
02	P1_REG_02	31: 0	0x8E89BED6	-	-
	ACCESS_ADDRESS	31: 0	0x8E89BED6	R/W	Access Address setting in BLE mode: Advertising package: always be 0x8e89bed6. Packet: Connections in link lay are all different.
03	P1_REG_03	15: 0	0x0000	-	-
	DEV_COM_POS	15: 0	0x0000	R/W	Overall directional frequency deviation adjustment, which is upward adjustment value. Step value is: 2M mode: Step value is about 4KHz;

					1M mode: Step value is about 514Hz;
04	P1_REG_04	15: 0	0x0000	-	-
	DEV_COM_NEG	15: 0	0x0000	R/W	Overall directional frequency deviation adjustment, which is downward adjustment. Step value is: 2M mode: Step value is about 4KHz; 1M mode: Step value is about 514Hz;
05	P1_REG_05	7: 0	0x35	-	RX Path
	Reserved	7	0	-	-
	OTA_VSEL<2: 0>	6: 4	011	R/W	Control of mixer OTA DC operating point: 1.044~1.376
	MIX_ISEL<1: 0>	3: 2	01	R/W	Control of mixer reference current.
	MIX_RSEL<1: 0>	1: 0	01	R/W	Control of mixer output DC operating point.

10 Application Reference Diagram

10.1 SOP8 application reference diagram

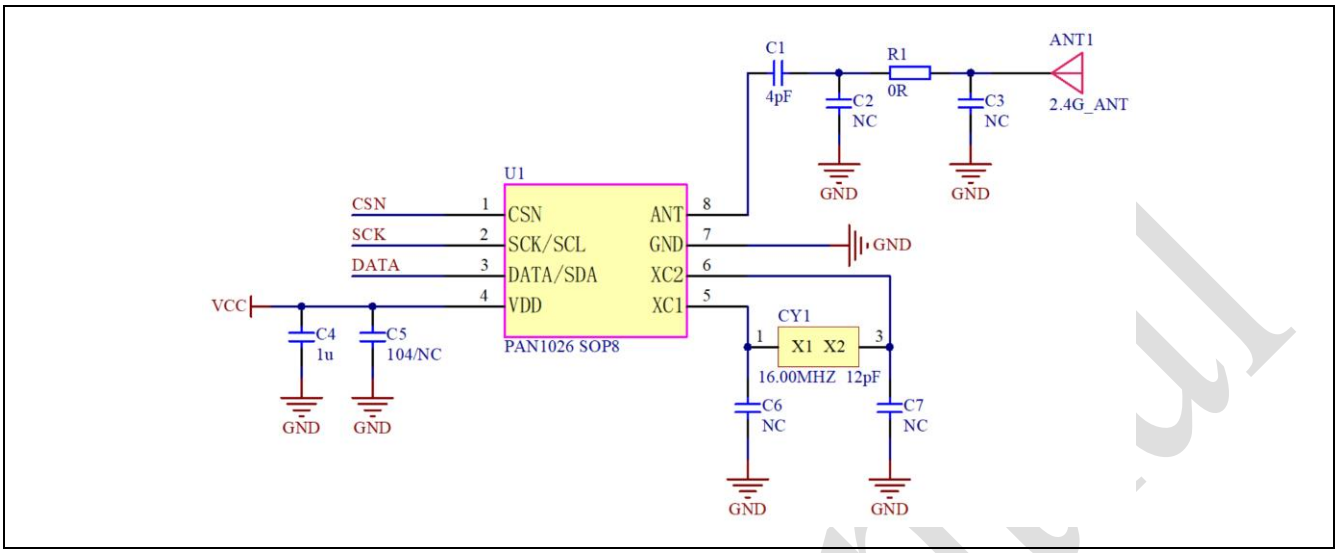


Figure 10-1 SOP8 application reference diagram

10.2 QFN16 application reference diagram

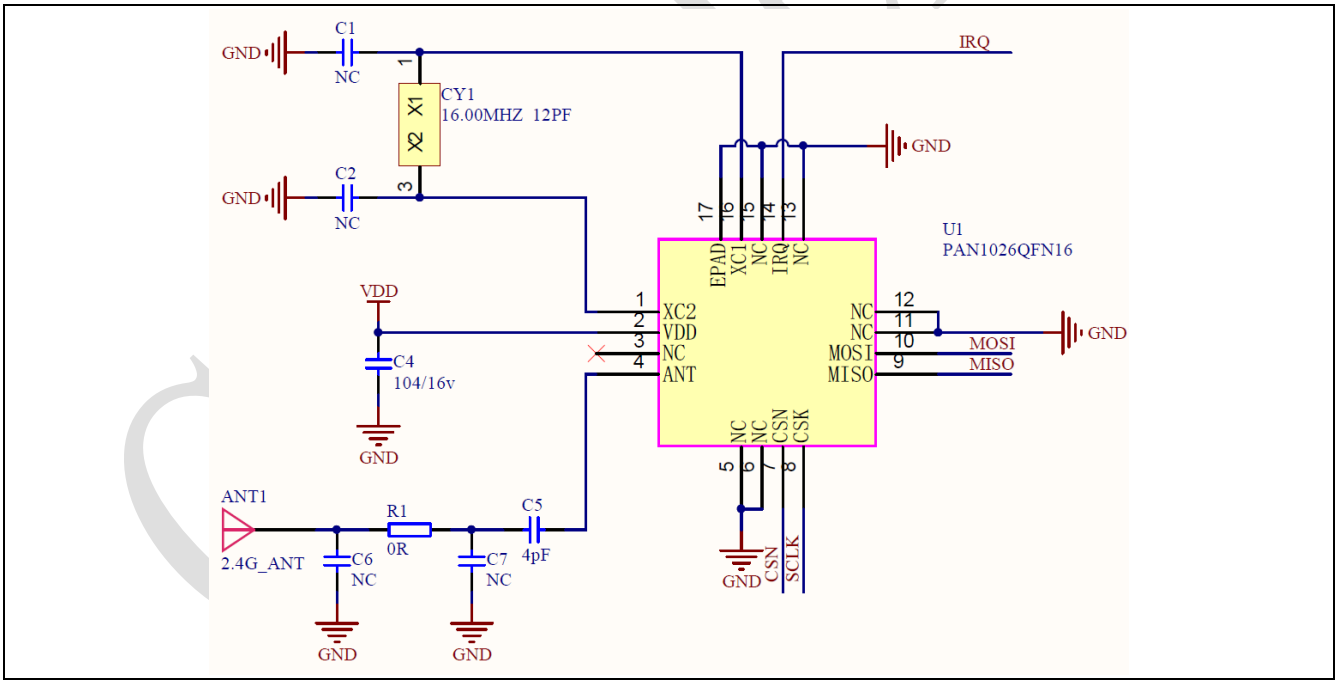


Figure 10-2 QFN16 application reference diagram

Note: Since the load capacitor of the crystal is shrunk inside the chip, the internal load capacitor cannot be adapted to all the crystals. The crystal should be selected according to “PAN1026 Hardware Design Reference”.

11 Package Dimensions

11.1 SOP8 package

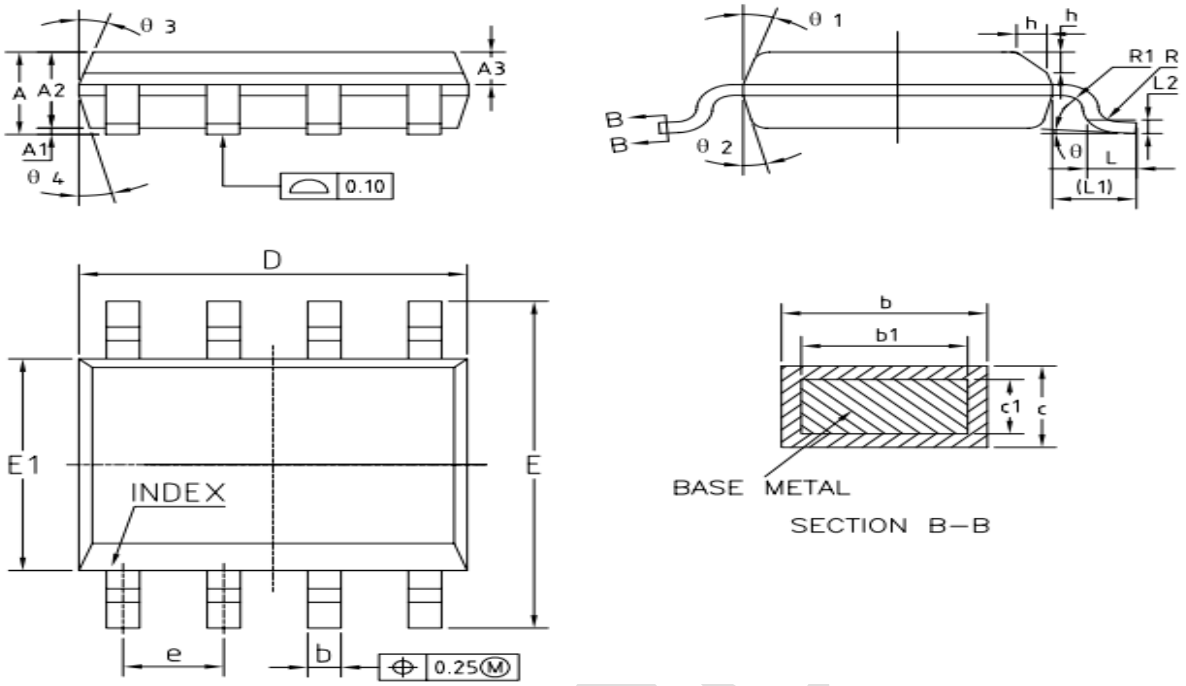


Figure 11-1 SOP8 Package View

Table 11-1 SOP8 Package Dimension

Symbol	Min.	Typ.	Max
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	-	-

R1	0.07	-	-
h	0.30	0.40	0.50
Ø	0°	-	8°
Ø1	15°	17°	19°
Ø2	11°	13°	15°
Ø3	15°	17°	19°
Ø4	11°	13°	15°

Note 1: The unit of measurement is millimeters.

11.2 QFN16 package

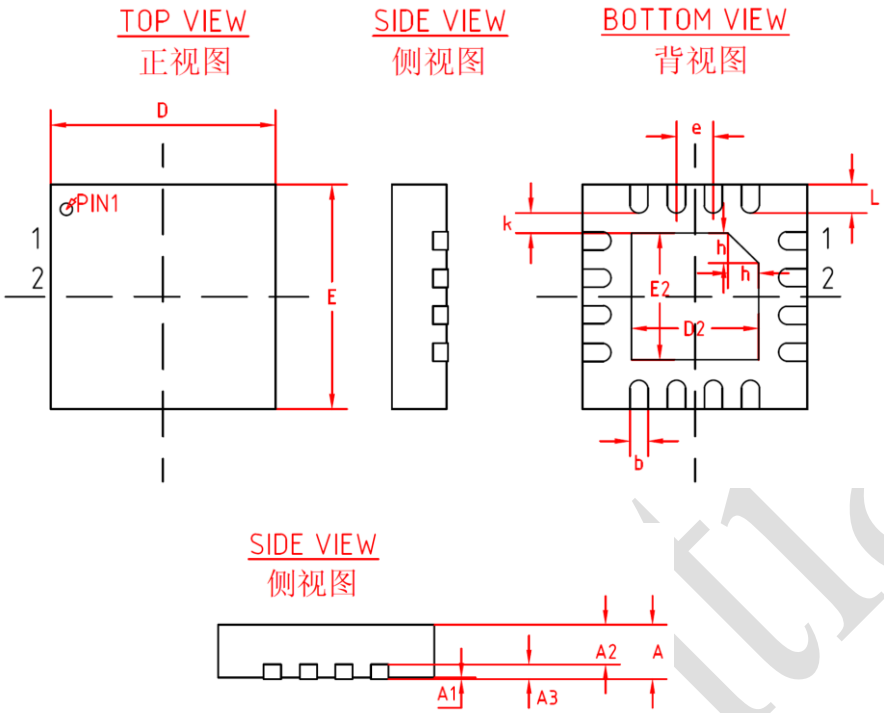


Figure 11-2 QFN16 Package View

Table 11-2 QFN16 Package Dimension

Symbol	Min.	Typ.	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203REF		
b	0.18	0.24	0.30
D	3BSC		
E	3BSC		
e	0.50BSC		
D2	1.6	1.7	1.8
E2	1.6	1.7	1.8
K	0.20BCS		
L	0.30	0.40	0.50
h	0.35	0.40	0.45

12 Precautions

1) This product is a CMOS device and should be protected against static electricity during storage, transportation and use.
2) Grounding when device is in use.
3) Reflow temperature can not exceed 260℃.

   The lead-free reflow soldering process is shown in the figure below:

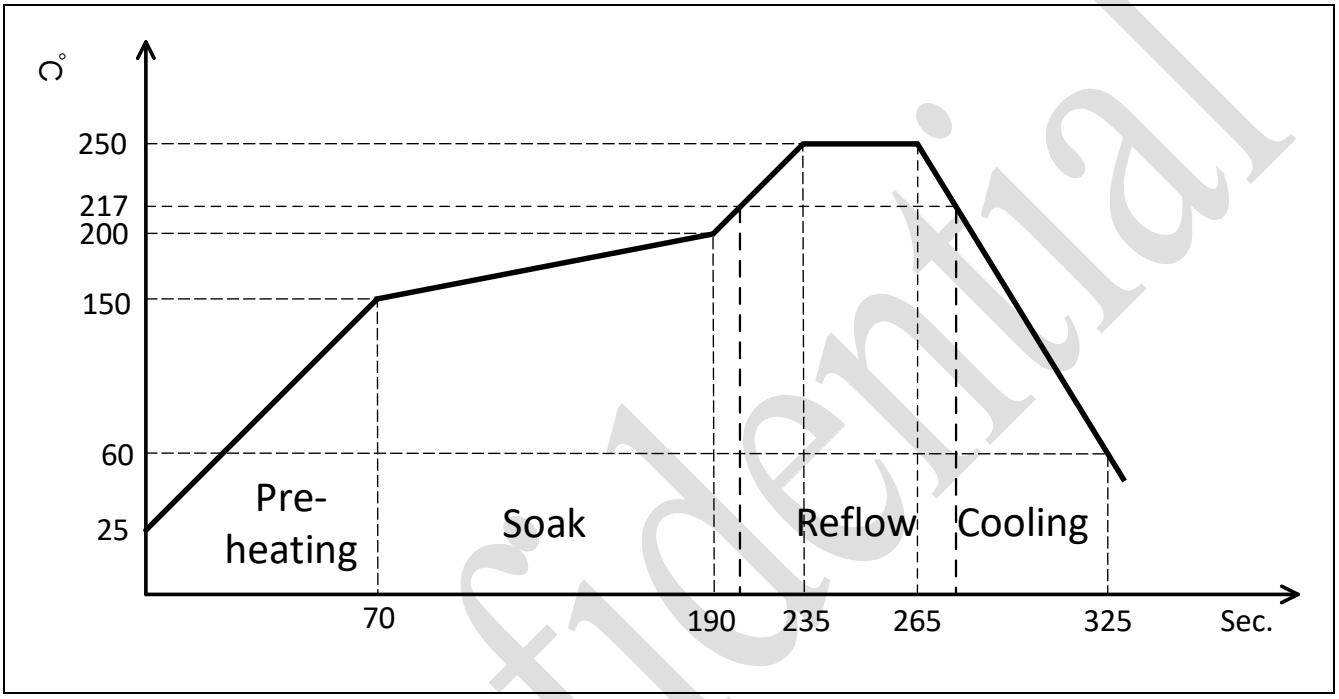


Figure 12-1 Reflow Profile

13 Storage Conditions

1) Products should be stored in sealed packages: when the temperature is less than 30 degrees and the humidity is less than 90%, it can last for 12 months.
2) After the package is opened, the components will be used in the reflow process or other high-temperature processes. The following conditions must be met:
   a) Completed within 72 hours and the factory environment is less than 30℃≤ 60% RH.
   b) Stored in 10% RH environment.
   c) Exhaust at 125℃ for 24 hours to remove internal water vapor before used.
3) MSL (Moisture Sensitivity Level): Level-3 (based on IPC/JEDEC J-STD-020)