Panchip Microelectronics Co., Ltd.

PAN3020

Datasheet

Sub-1GHz RF Transceiver

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REVISION HISTORY

Version	Date	Content	Reference
V1.0	2016.09	Initial	-
V1.1	2021.07	Update Application Reference Diagram and the corresponding recommended match parameters	-
V1.2	2022.06	Update Application Reference Design	-
V1.3	2023.07	Update Application Reference Design	-

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Abbreviation

ACK	Acknowledge Signal
BER	Bit Error Rate
CRC	Cyclic Redundancy Check
FEC	Forward Error Correction Code
FIFO	First Input First Output
GFSK	Gauss frequency Shift Keying
ISM	Industrial, scientific and medical bands
MCU	Microcontroller Unit
PID	Packet identification
PRX	Primary Receiver
PTX	Primary Transmitter
RF	Radio Frequency

1 General Description

PAN3020 is a single-chip wireless transceiver chip that works in multiple frequency bands below 1GHz, such as 315MHz / 433MHz / 868MHz / 915MHz (hereinafter referred to as 315 frequency band, 433 frequency band, 868 frequency band and 915 frequency band) general ISM frequency band.

PAN3020 chip integrates functional modules such as RF transceiver, frequency synthesizer, crystal oscillator, modem, etc., and supports one-to-many networking and communication mode with ACK. PAN3020 adopts GFSK modulation, and transmit output power, working channel and communication data rate can be configured.

1.1 Key Features

- RF
  - Frequency band: 315MHz / 433MHz / 868MHz / 915MHz
  - Data rate: 40Kbps, 80Kbps, 200Kbps, 400Kbps
  - Modulation: GFSK
- RF Synthesizer
  - Fully integrated synthesizer
  - Accept low cost ±10ppm crystal oscillator for the mode of 16MHz
- Transmitter
  - Transmitter output power is up to 20dBm
- Receiver
  - -112dBm@40Kbps；
  - -109dBm@80Kbps；
  - -106dBm@200Kbps；
  - -103dBm@400Kbps
- Protocol Engine
  - Support 1~ 32/64 bytes payload data
  - Data automatic verification
  - Support automatic retransmission and ACK
  - Built-in temperature detection function
- Power Management
  - Integrated voltage regulator
  - Operating voltage range: 2.2~3.3V
- Host Interface
  - Support FEC

- Support continuous transmission mode
- Up to 8Mbps SPI interface rate

- Package
  - SOP16
  - QFN20

1.2 Typical Applications

- Remote control
- Industrial control
- Wireless voice
- Smart home
- Security system

2 Block Diagram

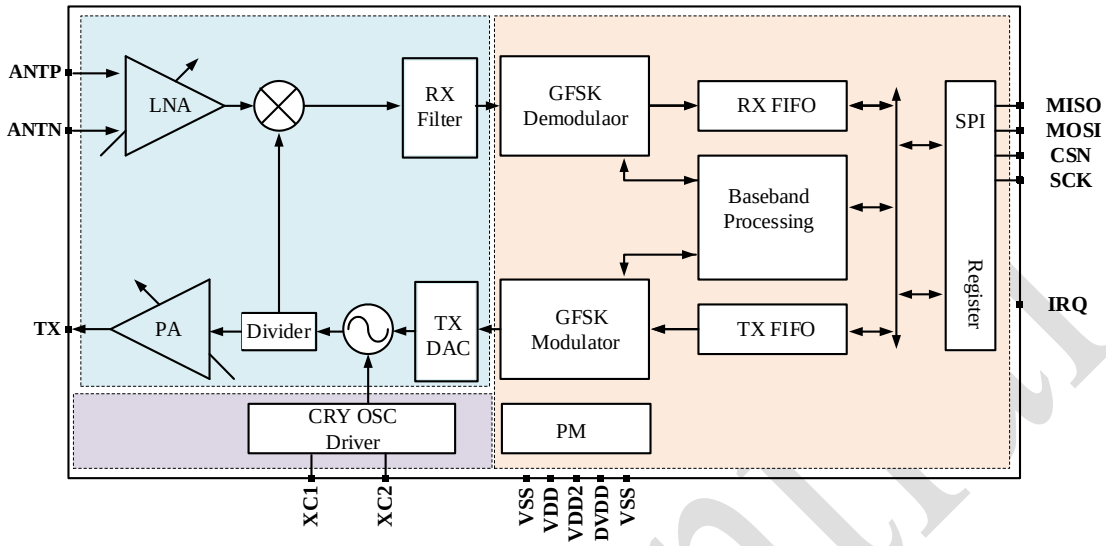

Figure 2-1 Block Diagram

3 Pin Information

3.1 Pin Diagram

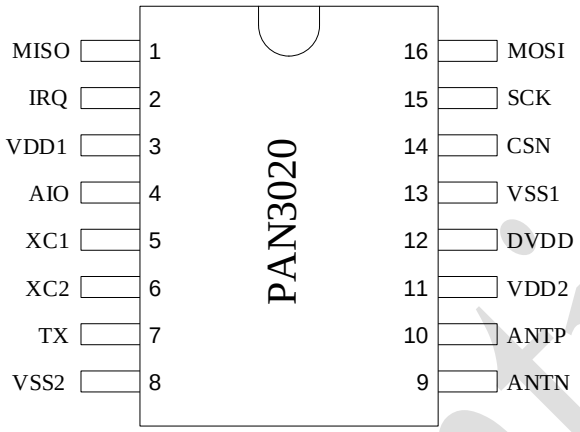

Figure 3-1 SOP16 Diagram

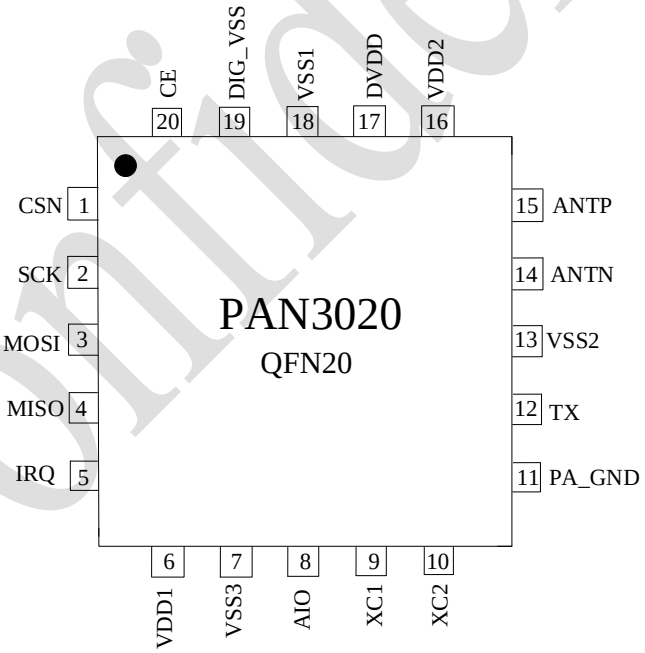

Figure 3-2 QFN20 Diagram

3.2 Pin Description

Table 3-1 SOP16 Pin Descriptions

No.	Sym.	Function	No.	Sym.	Function
1	MISO	SPI data output signal	9	ANTN	RF input
2	IRQ	Interrupt signal	10	ANTP	RF input
3	VDD1	Power supply input	11	VDD2	Power supply input
4	AIO	Analog signal input and output	12	DVDD	Internal voltage output
5	XC1	Crystal oscillator input	13	VSS1	Ground
6	XC2	Crystal oscillator output	14	CSN	The chip select signal of SPI
7	TX	RF output	15	SCK	The clock signal of SPI
8	VSS2	Ground	16	MOSI	SPI data input signal

Table 3-2 QFN20 Pin Descriptions

No.	Sym.	Function	No.	Sym.	Function
1	CSN	The chip select signal of SPI	11	PA_GND	Ground
2	SCK	The clock signal of SPI	12	TX	RF output
3	MOSI	SPI data input signal	13	VSS2	Ground
4	MISO	SPI data output signal	14	ANTN	RF input
5	IRQ	Interrupt signal	15	ANTP	RF input
6	VDD1	Power supply input	16	VDD2	Power supply input
7	VSS3	Ground	17	DVDD	Internal voltage output
8	AIO	Analog signal input and output	18	VSS1	Ground
9	XC1	Crystal oscillator input	19	DIG_VSS	Ground
10	XC2	Crystal oscillator output	20	CE	Mode chip select signal

4 Electrical Specification

4.1 Absolute Maximum Ratings

Table 4-1 Absolute maximum ratings

Symbol	Parameter(Condition)	Min	Max	Units
V_{DD}	Supply voltage	-0.3	3.6	V
V_I	Input voltage	-0.3	5	V
V_O	Output voltage	VSS	VDD	-
Pd	Total Power Dissipation （TA=-40℃~85℃）	-	400	mW
T_{OP}	Operating Temperature	-40	125	℃
T_{STG}	Storage Temperature	-40	140	℃

Note:

- Exceeding one or more of the limiting values may cause permanent damage to PAN3020.
- Electrostatic sensitive devices, observe the protective rules when handling.

4.2 Current Consumption

Table 4-2 Current Consumption

Symbol	Parameter (Condition)	Min	Typ	Max	Unit
ICC	Power-down	-	2	-	uA
	Standby I	-	50	-	uA
	Standby II	-	750	-	uA
	TX mode (1dBm)	-	20	-	mA
	TX mode (8dBm)	-	30	-	mA
	TX mode (15dBm)	-	50	-	mA
	TX mode (20dBm)	-	85	-	mA
	RX mode (DR=400Kbps)	-	18	18.5	mA
	RX mode (DR=200Kbps)	-	18	18.5	mA
	RX mode (DR=80Kbps)	-	18	18.5	mA
	RX mode (DR=40Kbps)	-	18	18.5	mA

4.3 General RF Conditions

Table 4-3 General RF Conditions

Symbol	Parameter(Condition)	Min	Typ	Max	Unit
f_{OP}	Operating Frequency （315 frequency band）	270	-	360	MHz
	Operating Frequency （433 frequency band）	400	-	550	MHz
	Operating Frequency （868/915 frequency band）	800	-	1100	MHz
PLL_{res}	PLL Programming Resolution	-	20	-	KHz
f_{XTAL}	Crystal Frequency	-	16	-	MHz
DR	Data Rate	-	40	-	Kbps
		-	80	-	Kbps
		-	200	-	Kbps
		-	400	-	Kbps
Δf	Frequency Deviation @40Kbps	-	20	-	KHz
	Frequency Deviation @80Kbps	-	40	-	KHz
	Frequency Deviation @200Kbps	-	100	-	KHz
	Frequency Deviation @400Kbps	-	200	-	KHz
FCH	Channel Spacing @40Kbps	-	120	-	KHz
	Channel Spacing @80Kbps	-	240	-	KHz
	Channel Spacing @200Kbps	-	600	-	KHz
	Channel Spacing @400Kbps	-	1200	-	KHz

4.4 Transmitter Operation

Table 4-4 Transmitter Operation

Symbol	Parameter(Condition)	Min	Typ	Max	Unit
PRF	Typical Output Power	-	15	-	dBm
$PRFC$	Output Power Range （315/433 frequency band）	-70	-	20	dBm
	Output Power Range （868/915 frequency band）	-70	-	15	dBm
PBW	20dB Bandwidth For Modulated Carrier at 40Kbps	-	80	-	KHz
	20dB Bandwidth For Modulated Carrier	-	160	-	KHz

	at 80Kbps				
	20dB Bandwidth For Modulated Carrier at 200Kbps	-	400	-	KHz
	20dB Bandwidth For Modulated Carrier at 400Kbps	-	800	-	KHz

4.5 Receiver Operation

Table 4-5 Receiver Operation

Symbol	Parameter(Condition)	Min	Typ	Max	Unit
RX_{max}	Maximum Received Amplitude at <0.1% BER	-	0	-	dBm
RXSENS	Sensitivity（0.1%BER，DR=40Kbps，△f=±20KHz，@433 frequency band）	-	-112	-	dBm
	Sensitivity（0.1%BER，DR=80Kbps，△f=±40KHz，@433 frequency band）	-	-109	-	dBm
	Sensitivity（0.1%BER，DR=200Kbps，△f=±100KHz，@433 frequency band）	-	-106	-	dBm
	Sensitivity（0.1%BER，DR=400Kbps，△f=±200KHz，@433 frequency band）	-	-103	-	dBm
	Sensitivity（0.1%BER，DR=40Kbps，△f=±20KHz，@315 frequency band）	-	-112	-	dBm
	Sensitivity（0.1%BER，DR=80Kbps，△f=±40KHz，@315 frequency band）	-	-109	-	dBm
	Sensitivity（0.1%BER，DR=200Kbps，△f=±100KHz，@315 frequency band）	-	-106	-	dBm
	Sensitivity（0.1%BER，DR=400Kbps，△f=±200KHz，@315 frequency band）	-	-103	-	dBm
	Sensitivity（0.1%BER，DR=40Kbps，△f=±20KHz，@868 frequency band）	-	-107	-	dBm
	Sensitivity（0.1%BER，DR=80Kbps，△f=±40KHz，@868 frequency band）	-	-104	-	dBm
	Sensitivity （0.1%BER， DR=200Kbps， △f=±100KHz, @868 frequency band）	-	-101	-	dBm
	Sensitivity（0.1%BER，DR=400Kbps，△f=±200KHz，@868 frequency band）	-	-98	-	dBm
	Sensitivity（0.1%BER，DR=40Kbps，△f=±20KHz，@915 frequency band）	-	-107	-	dBm
	Sensitivity（0.1%BER，DR=80Kbps，△f=±40KHz，@915 frequency band）	-	-104	-	dBm
	Sensitivity（0.1%BER，DR=200Kbps，△f=±100KHz，	-	-101	-	dBm

	@915 frequency band）				
	Sensitivity（0.1%BER，DR=400Kbps，△f=±200KHz，@915 frequency band）	-	-98	-	dBm
C/I_{CO}	C/I Co-Channel @40Kbps	-	13	-	dBc
C/I_{1ST}	1st Adjacent Channel Selectivity @40Kbps	-	-21	-	dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity @40Kbps	-	-35	-	dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity @40Kbps	-	-43	-	dBc
C/I_{CO}	C/I Co-Channel @80Kbps	-	13	-	dBc
C/I_{1ST}	1st Adjacent Channel Selectivity @80Kbps	-	-20	-	dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity @80Kbps	-	-33	-	dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity @80Kbps	-	-42	-	dBc
BLOCK	Deviation from 1MHz blocking @40Kbps	-	-53	-	dBc
	Deviation from 4MHz blocking @40Kbps	-	-57	-	dBc
	Deviation from 8MHz blocking @40Kbps	-	-65	-	dBc
IR	Image Suppression	-	-30	-	dBc

4.6 DC Characteristics

Table 4-6 DC Characteristics

Symbol	Parameter(Condition)	Min	Typ	Max	Unit
VDD	Supply Voltage	2.2	3	3.3	V
VSS	Ground	-	0	-	V
V_{OH}	Output High Level Voltage	VDD-0.3	-	VDD	V
V_{OL}	Output Low Level Voltage	VSS	-	VSS+0.3	V
V_{IH}	Input High Level Voltage	VDD-0.3	-	VDD	V
V_{IL}	Input Low Level Voltage	VSS	-	VSS+0.3	V

5 Operational Modes

This chapter describes all kinds of operating modes of PAN3020 and the methods used to control the chip into each mode of operation. PAN3020 chip's own state machine is controlled by the configuration values of the chip's internal registers and external pin signals.

5.1 State Diagram

The state diagram in Figure 5-1 shows 6 kinds of operating modes and how they jump. The PAN3020 starts to work normally when VDD is greater than 2.2V. Even if it enters power down mode, the MCU can send configuration commands through the SPI and CE pins to put the chip into the other states.

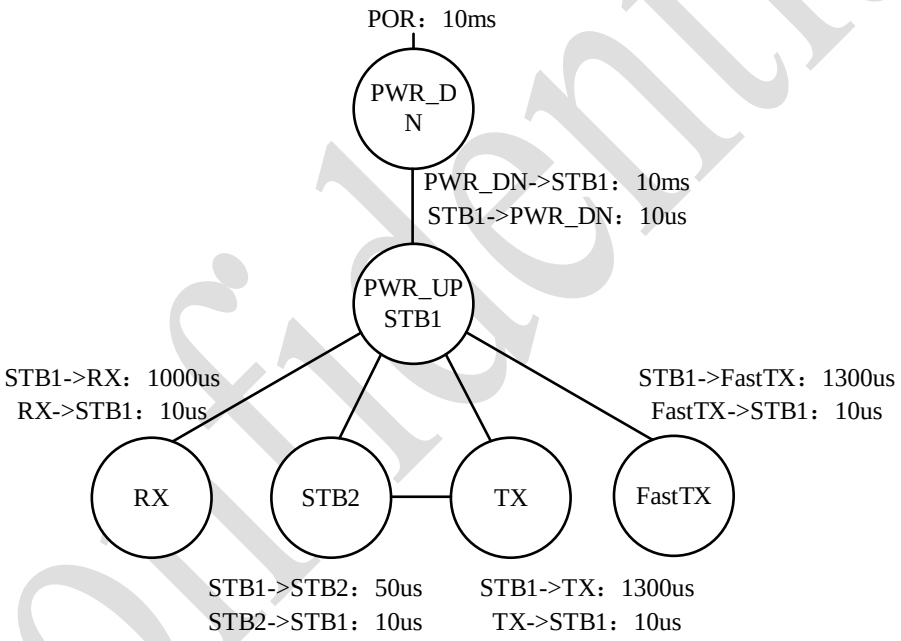

Figure 5-1 State diagram

PAN3020 has 6 kinds of operating modes, power down mode (PWR_DN), standby mode-I (STB1), standby mode-II (STB2), receive mode (RX), transmit mode (TX) and continuous transmit mode (FastTX).

5.2 Operational Modes Configuration

The Table 5-1describes how to configure the operational modes and the functions.

Table 5-1 PAN3020 operational modes

MODE		PWR_DN	STB1	STB2	RX	TX	FastTX
CONTROL BIT	PWR_UP	0	1	1	1	1	1
	CE	0	0	1	1	1	1
	PRIM_RX	X	X	0	1	0	0
	FAST_MODE	X	X	X	X	0	1
FUNCTION DESCRIPTION	SPI Operation	√	√	√	√	√	√
	Keep Register Value	√	√	√	√	√	√
	Crystal Oscillator Work	X	√	√	√	√	√
	Crystal Oscillator Output	X	X	√	√	√	√
	Enable Power Management Module	X	X	√	√	√	√
	Enable TX Module	X	X	X	X	√	√
	Enable RX Module	X	X	X	√	X	X

5.3 Power Down Mode

In power down mode, all PAN3020 functions are turned off with a minimum current consumption. After entering power down mode, the PAN3020 stops working, but the contents of the registers remain unchanged. Power down mode is controlled by the PWR_UP bit in the register.

5.4 Standby-I Mode (STB1)

In standby-I mode, the chip maintains crystal oscillation but does not output to other modules. The other functional modules are turned off and the current consumption is small. The device enters to standby-I mode from power down mode by setting the PWR_UP bit in the CONFIG register to 1. In the transmit or receive mode, the chip can return to standby-I mode by setting the CE control signals to 0.

5.5 Standby-II Mode (STB2)

The standby-II mode can usually be understood as a preliminary transmission mode. The device enters to standby- II mode by setting the CE to 1 while the TX FIFO register is empty. At this time, the crystal oscillator has a strong output drive capability and the power management module of the chip is turned on. In standby-II mode, if a data packet is sent to the TX FIFO, the internal phase-locked loop (PLL) of the chip starts working immediately and after a lock time of the PLL, the transmitter transmits the data packet.

5.6 RX Mode

The device enters to RX mode by setting the PWR_UP, PRIM-RX, and CE to 1. In RX mode, the RF part receives the signal from the antenna, then amplifies, downconverts, filters and demodulates it.The packe's validity will be judged according to the address, check code, data length, etc. The valid pakege will be uploaded to the RX FIFO and trigger interruption. If the RX FIFO is full, the received packet will be discarded.

5.7 TX Mode

The device enters to TX mode by setting the PWR_UP and CE to 1, PRIM-RX to 0 while there is valid data in the TX FIFO. The PAN3020 remains in TX mode until the packet is sent. After the transmission is completed, the device returns to the standby mode. In the transmission mode of PAN3020, data packets are sent in a single packet.

5.8 Fast TX Mode

When the PWR_UP 1, CE pin has a pulse of 1 (from 0 to 1 and maintain more than 20us, then 0), PRIM-RX is set to 0, FAST_MODE 1, and there is valid data in the TX FIFO, continuous emission mode(FastTX) is entered.

When PAN3020 enters continuous emission mode, as long as there is data in the TX FIFO, it will remain in the sending state, and the data will continue to be sent one packet at a time; To return to standby mode-I, the MCU has to FAST_MODE 0 via SPI.

6 Packet format description

6.1 Packet Format for Normal BURST

The normal burst mode packet format is shown in Table 6-1, framing mode I.

In the address and data part of Table 6-1, the scrambling mode can be selected, according to the enable/disable scrambling code configuration bit.

Table 6-1 Packet format for Normal BURST

Preamble (3 bytes)	Address (3~5 bytes)	Payload (1~32/64 bytes)	CRC (0/1/2 bytes)

6.2 Packet Format for Enhanced BURST

The enhanced burst mode packet format is shown in Table 6-2, framing mode II.

In the address, identification and data part of Table 6-2, the scrambling mode can be selected, according to the enable/disable scrambling code configuration bit.

Table 6-2 Packet format for Enhanced BURST

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			Payload (0~32/64 byte)	CRC (0/1/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)		

6.3 ACK Packet Format for Enhanced BURST

The ACK Packet format for Enhanced BURST is shown in Table 6-3, framing mode III.

The address and identification part of Table 6-3 need to select the same enable/disable scrambling mode as PTX.

Table 6-3 ACK Packet format for Enhanced BURST

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			CRC (0/1/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)	

7 Data Communication Modes

The communication modes of PAN3020 can be classified into two kinds:

- Without automatic retransmission without ACK communication mode (Normal BURST), the transmitter can use commands such as W_TX_PAYLOAD, REUSE_TX_PL, etc. Continuous emission mode(FastTX) belongs to Normal BURST.
- With automatic retransmission with ACK communication mode (Enhanced BURST), the transmitter can use commands such as W_TX_PAYLOAD, W_TX_PAYLOAD_NOACK, REUSE_TX_PL, etc. The receiver can use commands such as W_ACK_PAYLOAD, etc.

Table 7-1 Normal BURST

Communication Name	**Normal BURST**	
Communication Party	PTX	Communication Party
Feature	One Way Transmit	Feature
Framing Method of Transmiting Data	I	Framing Method of Transmiting Data
Start Command REUSE_TX_PL	Re-Transmit the Previous Packet	Start Command REUSE_TX_PL

Table 7-2 Enhanced BURST

Communication Name	**Enhanced BURST**	
Communication Party	PTX	PRX
Feature	After transmiting data, wait for receiving ACK	After receiving the data, send back ACK
Framing Method Of Transmiting Data	Send data framing mode II	Send back ACK framing mode III
PTX using the REUSE_TX_PL command	Re-Transmit The Previous Packet	Once receive a packet, send back ACK
PTX using the W_TX_PAYLOAD command PRX using the W_ACK_PAYLOAD command	After transmiting data, wait to receive ACK PAYLOAD	After receiving data, send back ACK PAYLOAD, framing mode II
PTX using the W_TX_PAYLOAD_NO_ACK command	Transmit data once, not waiting for ACK, framing mode II	Receive data, do not return ACK

7.1 Normal BURST

In normal mode, the sender fetches data from the TX FIFO register and sends it. After the transmission is completed, the interrupt is reported (interrupt needs to be cleared), and the TX FIFO register clears the data (the TX FIFO needs to be cleared), the receiver receives a valid address and data. The MCU is notified of the interrupt, and the MCU can then read the data from the RX FIFO register (the TX FIFO, RX FIFO and interrupt all need to be cleared).

In Normal BURST, (0X01) EN_AA register is set to 0X00, (0X04) SETUP_RETR register is set to 0X00, (0X1C) DYNPD register is set to 0X00, The lower 3 bits of the (0X1D)FEATURE register are set to 000.

7.2 Enhanced BURST

In the enhanced burst, the party that initiates the communication is called PTX (the primary originating terminal), and the party that receives the data and responds is called the PRX (the primary receiving terminal). After the PTX sends the data, it waits for the response signal, and the PRX returns the response signal after receiving the valid data. If the PTX does not receive an acknowledgement signal within the specified time, it automatically resends the data. The automatic retransmission and auto answer functions are included with the PAN3020 chip and do not require MCU participation.

PTX automatically transfers to the TX mode waiting response signal after transmitting data. If the correct response signal is not received within the specified time, the PTX will resend the same data packet until the acknowledge signal is received, or the number of transmissions exceeds the ARC value (SETUP_RETR register) to generate the MAX_RT interrupt. The PTX receives the acknowledgement signal, that is, the data has been successfully transmitted (PRX receives valid data).Then the data in the TX FIFO are cleared and a TX_DS interrupt is generated (the TX FIFO and RX FIFO need to be cleared, and the interrupt needs to be cleared).

Each time PRX receives a valid data packet, it will return an ACK response signal. If the data is new data (the PID value is different from the previous packet data), it will be saved to the RX FIFO, otherwise it will be discarded.

In enhanced mode, it is necessary to ensure that the TX address of the PTX (TX_ADDR), the RX address of channel 0 (such as RX_ADDR_P0), and the RX address of the PRX (such as RX_ADDR_P5) are the same. For Example: In Figure 7-5, PTX5 corresponds to the data channel 5 of PRX, and the address is set as follows:

- PTX5：TX_ADDR=0xC2C3C4C5C1
- PTX5：RX_ADDR_P0=0xC2C3C4C5C1
- RX：RX_ADDR_P5=0xC2C3C4C5C1

Enhanced burst has the following characteristics:

- Reduce MCU control and simplify software operation.
- Strong anti-interference ability, reduce packet loss caused by instantaneous co-channel interference in wireless transmission, and easier to develop frequency hopping algorithm.
- During the retransmission process, reduce the operation time of the MCU each time to write data to be sent through the SPI interface.

7.3 Enhanced TX Mode

1. CE is set to 0, the PRIM_RX bit of the CONFIG register is set to 0.

2. When transmitting data, the transmit address (TX_ADDR) and valid data (TX_PLD) are written to the address register and the TX FIFO in bytes via the SPI interface. When the CSN pin is low, data is written, the CSN pin is set to high again, and the data write operation completes.
3. CE is set to 1 from 0, the transmission is started (CE is kept 1 for more than 30us, the operation takes effect).
4. In automatic reply mode (SETUP_RETR register is not set to 0, ENAA_P 0 = 1), PTX automatically switches channel 0 to RX mode to wait for the reply signal immediately after sending the data. If an ACK response signal is received within the valid response time range, the data is considered to have been sent successfully, and the TX_DS position of the status register is 1 and the data in the TX FIFO is automatically cleared. If the response signal is not received within the set time range, the data is automatically retransmitted.
5. If the automatic transfer counter (ARC_CNT) overflows (exceed the set value), the MAX_RT bit of the status register is set and the data in the TX FIFO is not cleared. When MAX_RT or TX_DS is 1, the IRQ pin generates a low interrupt (the corresponding interrupt needs to be enabled). Interrupts can be reset by writing to the status register.
6. The packet loss counter (PLOS_CNT) is incremented by one each time the MAX_RT interrupt is generated. The automatic transmission counter ARC_CNT counts the number of times the data packet is retransmitted; the packet loss counter PLOS_CNT counts the number of data packets that have not been successfully transmitted when the maximum number of allowed transmission times is reached.
7. After the MAX_RT or TX_DS interrupt is generated, the system enters standby mode.

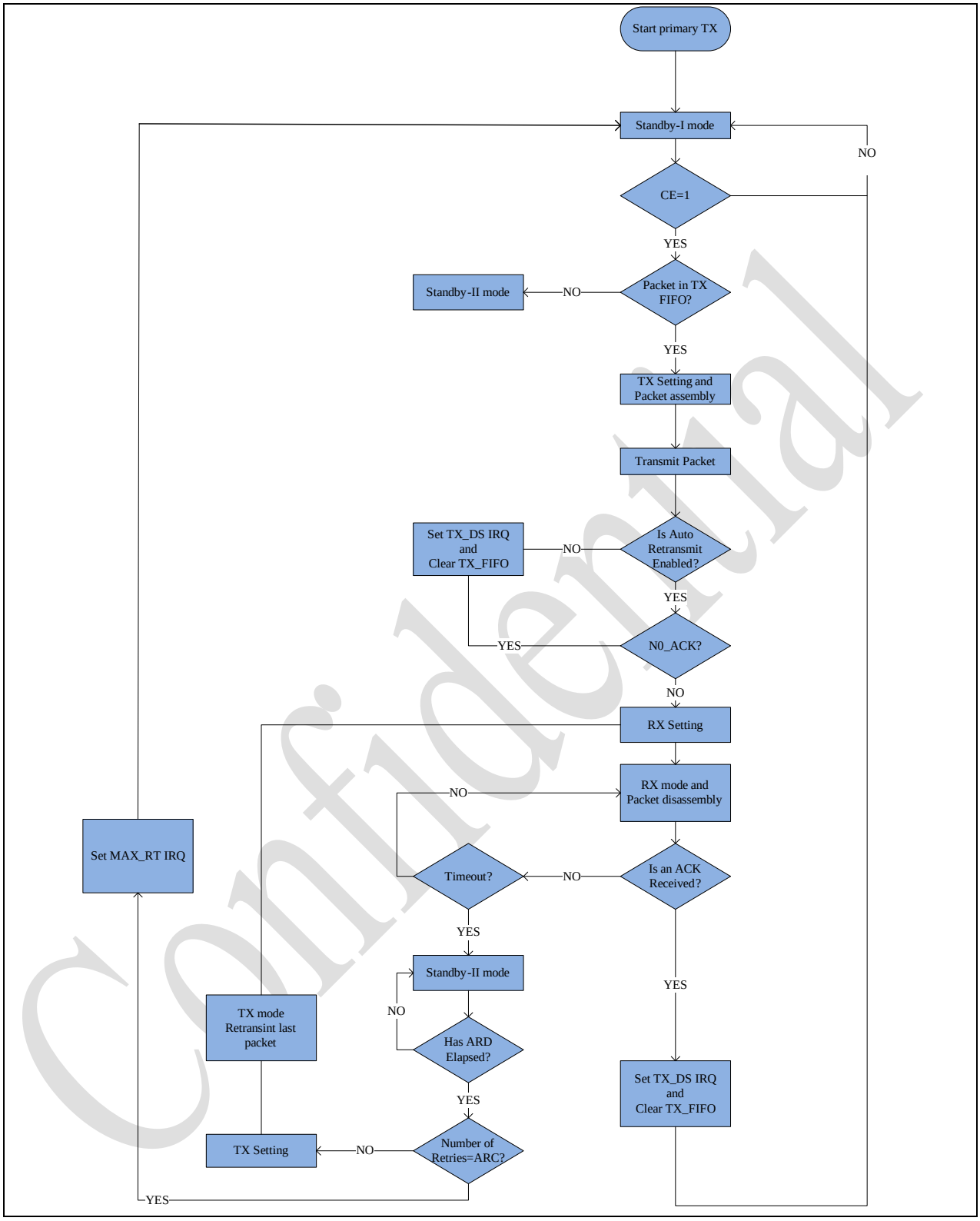

Figure 7-1 Enhanced sender processes

7.4 Enhanced RX Mode

1. When CE is set to 0, the PRIM_RX bit in the CONFIG register is set first. The channel ready to receive data must be enabled (EN_RXADDR register). All auto-answer functions for data channels operating in Enhanced BURST mode are enabled by the EN_AA register. The valid data width is set by the RX_PW_PX register.
2. RX mode is started by setting CE to 1.
3. After the preset waiting time, PRX starts to detect the wireless signal.
4. After receiving valid data packets, data is stored in RX_FIFO, and RX_DR bit is set to 1, resulting in an interruption. In the status register, the RX_P_NO bit shows which channel the data was received.
5. Automatic transmit ACK response signal.
6. If CE remains at 1, continue to enter receive mode, if CE is set to 0, enter standby mode-III.
7. The MCU reads the data through the SPI port at an appropriate rate.

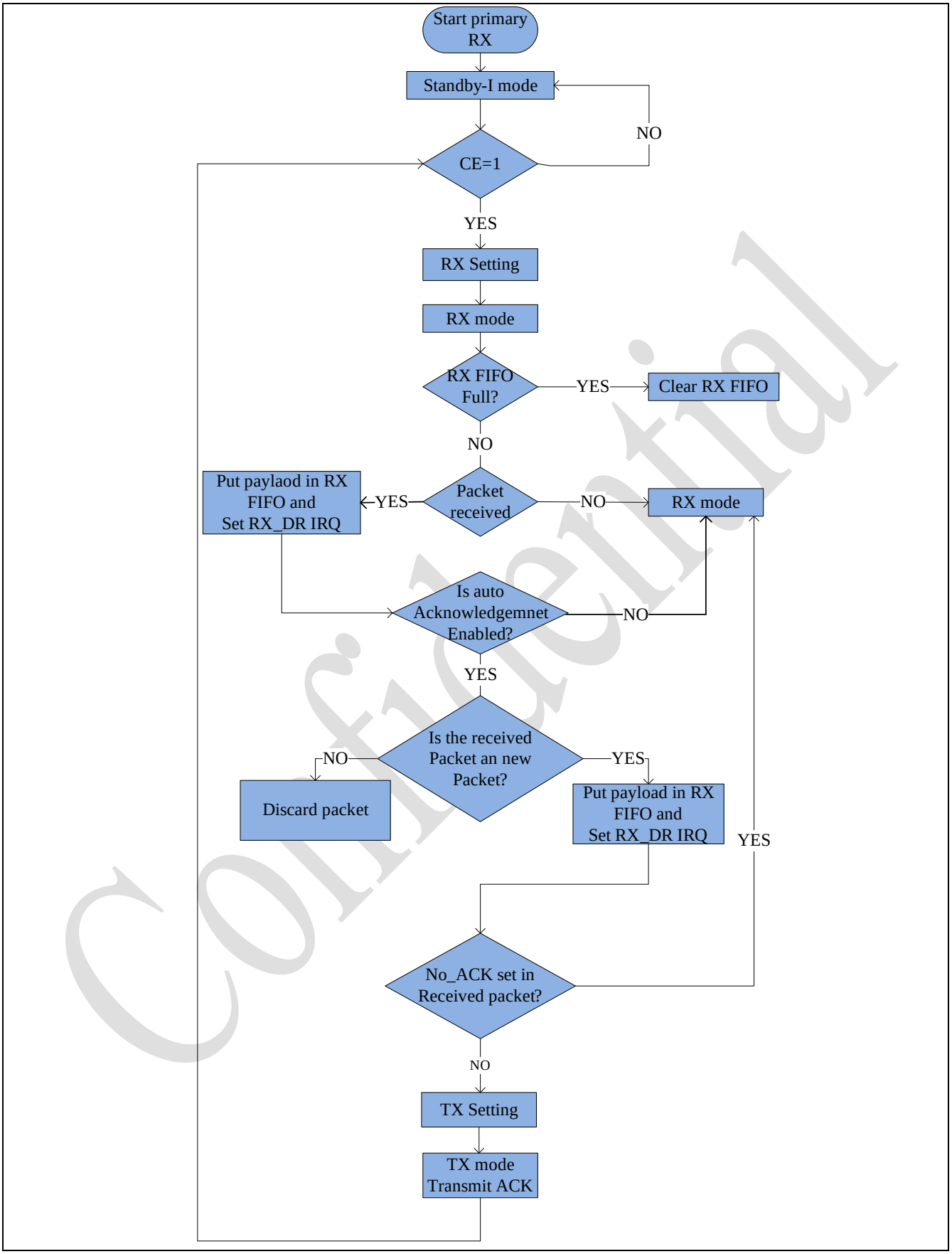

Figure 7-2 Enhanced receiver processes

7.5 Packet Identification in Enhanced BURST

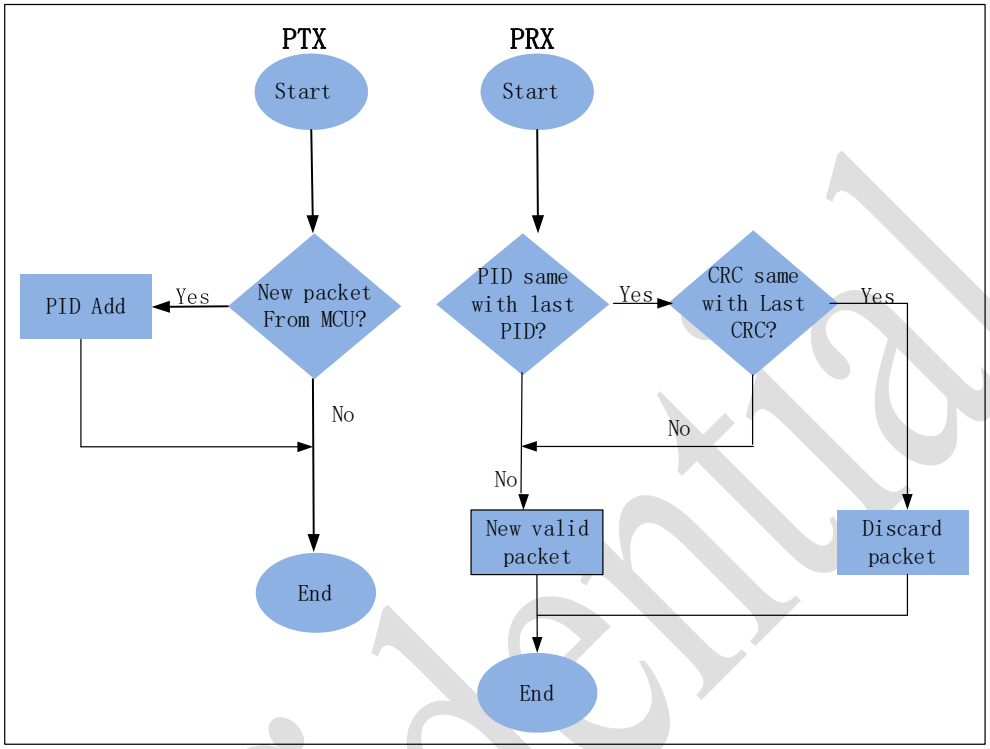

Figure 7-3 PID generation and detection

Each packet of data includes two PIDs (packet flag bits) to help the receiving terminal identify whether the data is new or retransmitted, preventing the same data packet from being stored multiple times. PID generation and detection is shown in Figure 7-3. The PID value adds 1 once the sender fetches a new packet from MCU.

7.6 The PTX and PRX Timing of Enhanced BURST

Figure 7-4 shows the internal timing diagram of the PTX and PRX communication. To make the communication successful must meet the following two conditions.

- Condition 1: The three periods sum of PTX (or PRX) transmit PLL stabilization + power amplifier enable + PLL open-loop is greater than the PLL stability time received by PRX (or PTX) 20us or more, thus ensuring that the time period in which the PTX (or PRX) transmits data is within the time period during which the PRX (or PTX) receives the data. That is:

  EX_PA_TIME + TX_SETUP_TIME + TRX_TIME > RX_SETUP_TIME +20us

  Condition 2: The four periods sum of PRX transmit ACK PLL stabilization + power amplifier enable + PLL open-loop+ transmiting ACK is less than the two periods sum of PTX receive PLL stabilization + wait ACK 80us or more, thus ensuring that the time period in which the PRX replies ACK is within the time period during which the PTX waits ACK. The time to send

the ACK is to send the number of frames bits ÷ the communication data rate. That is:

EX_PA_TIME + TX_SETUP_TIME + TRX_TIME + SEND_ACK_TIME <

RX_SETUP_TIME + RX_ACK_TIME - 80us

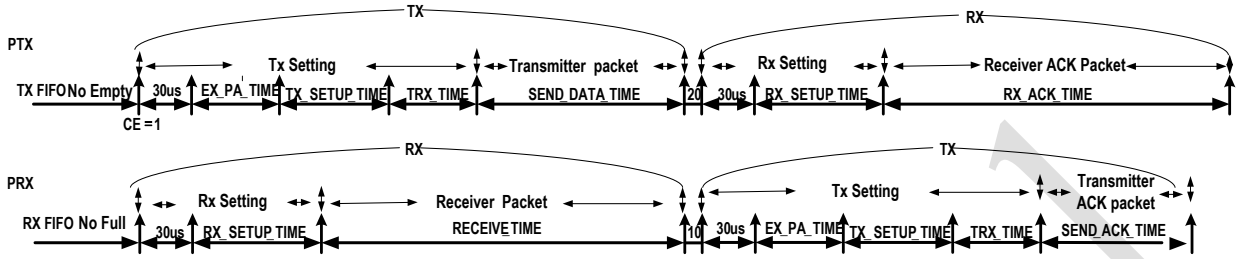

Figure 7-4 The timing of Enhanced BURST

7.7 One-To-Multi Communication at the Receiving End in Enhanced BURST

When the PAN3020 chip acts as a transmit terminal, different addresses can be used to communicate with multiple receiving eterminal for one-to-multi communication.

When the PAN3020 chip acts as a receive terminal, the PAN3020 chip can receive 6 channels of transmitter data with different addresses and the same frequency. Each data channel has its own address.

Which data channels are enabled are set by the register EN_RXADDR. The address of each data channel is configured by the register RX_ADDR_PX. Normally different data channels are not allowed to set the exact same address. As shown below, Table 7-3 gives an example of a multi-receive channel address configuration.

Table 7-3 Multi-channel address configuration

	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Data pipe 0(RX_ADDR_P0)	0xF1	0xD2	0xE6	0xA2	0x33
Data pipe 1(RX_ADDR_P1)	0xD3	0xD3	0xD3	0xD3	0xD3
Data pipe 2(RX_ADDR_P2)	0xD3	0xD3	0xD3	0xD3	0xD4
Data pipe 3(RX_ADDR_P3)	0xD3	0xD3	0xD3	0xD3	0xD5
Data pipe 4(RX_ADDR_P4)	0xD3	0xD3	0xD3	0xD3	0xD6
Data pipe 5(RX_ADDR_P5)	0xD3	0xD3	0xD3	0xD3	0xD7

It can be seen from Table 7-3 that the whole 40 bits addresses of 5 byte of data channel 0 are configurable, the address of data channel 1~5 is configured as 32-bit shared address (shared with data channel 1) + 8 bits of respective address (Lowest byte).

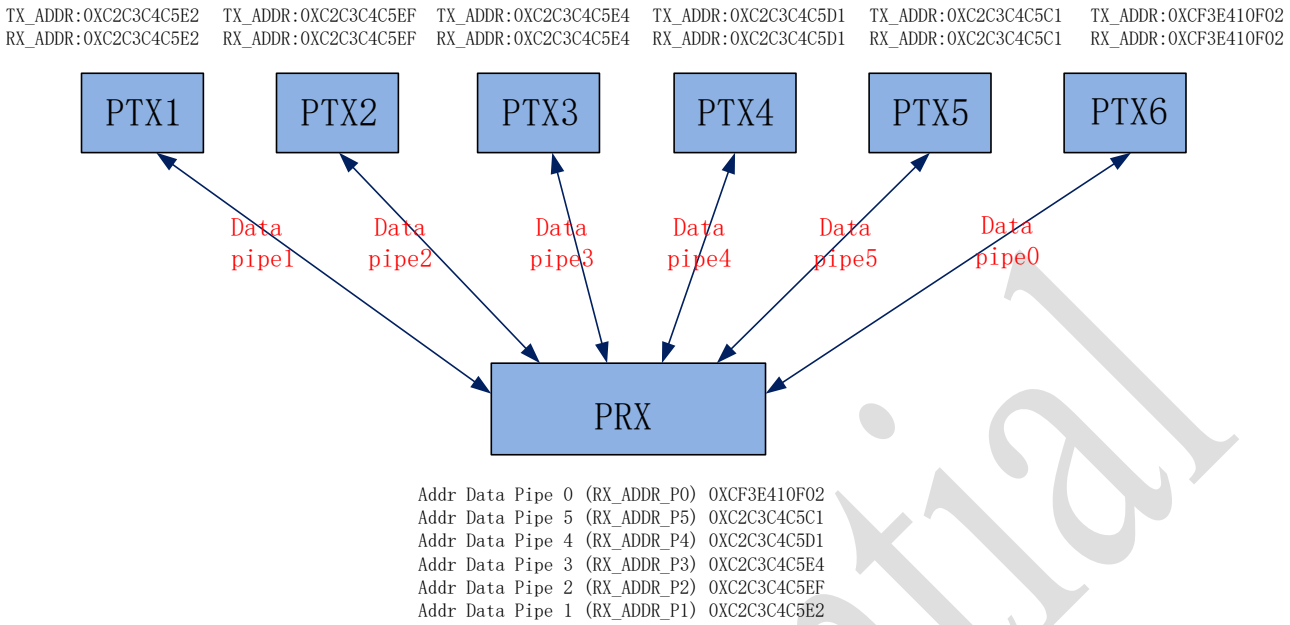

Figure 7-5 Example of data pipe addressing in star network

The PAN3020 chip can communicate with up to six different channels in RX mode, as shown in Figure 7-5. Each data channel uses a different address and shares the same channel. All transmitters and receivers are set to enhanced burst mode.

After receiving the valid data, the PRX records the TX address of the PTX and sends a response signal with the address as the target address. When PTX data channel 0 is used as the receive acknowledge signal, the RX address of data channel 0 is equal to the TX address to ensure that the correct acknowledge signal is received. Figure 7-5 shows an example of how PTX and PRX addresses are configured.

7.8 DATA FIFO

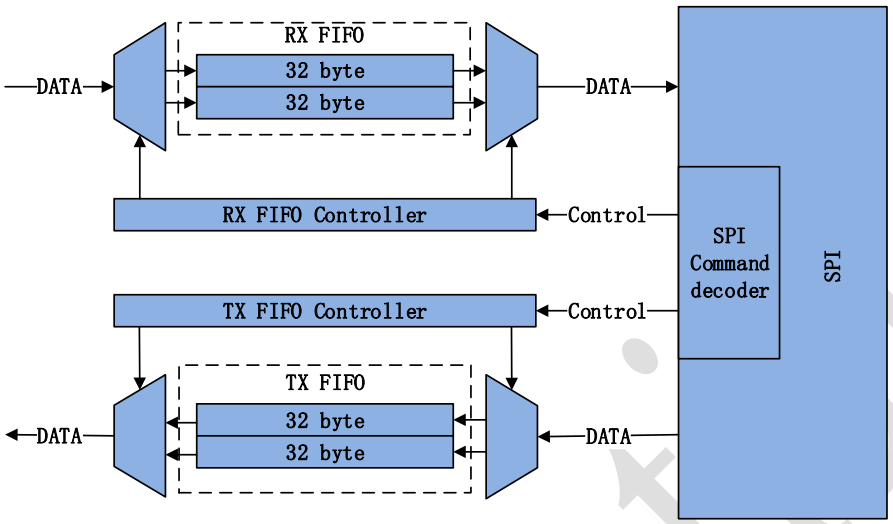

Figure 7-6 FIFO diagram

The PAN3020 chip is equipped with an MCU to complete the communication function together. The processing of the link layer, such as data framing, verification, address judgment, data whitening scrambling, data retransmission, and ACK response, is done internally by the chip without the involvement of the MCU.

The PAN3020 chip can be configured as two different RX FIFO registers (32 bytes) or one RX FIFO register (64 bytes) (shared by 6 receive channels), two different TX FIFO registers (32 bytes), or one TX FIFO register (64 bytes). In sleep mode and standby mode, the MCU can access FIFO registers.

The TX_FIFO is written by the W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK instructions in TX mode. The TX_DS or MAX_RT interrupt is generated and this packet of data in the TX_FIFO is cleared. In the RX mode, the payload in the RX_FIFO is read by the R_RX_PAYLOAD instruction, and the length of the payload is read by the R_RX_PL_WID instruction. The FIFO_STATUS register indicates the status of the FIFO.

7.9 Interrupt Pin

The interrupt pin (IRQ) of the PAN3020 chip is low-level triggered, the IRQ pin is initially high. When the TX_DS, RX_DR or MAX_RT in the status register is 1, and the corresponding interrupt reporting enable bit is 0, the interrupt of the IRQ pin is triggered. When the MCU writes '1' to the corresponding interrupt source, the interrupt is cleared. The IRQ pin interrupt trigger can be masked or enabled. By setting the interrupt report enable bit to 1, the interrupt trigger on the IRQ pin is disabled.

8 SPI Control Interface

The PAN3020 chip reads and writes to each register through the SPI control interface. The PAN3020 chip acts as a slave. The data rate of the SPI interface generally depends on the interface speed of the MCU, and its maximum data transfer rate is 8 Mbps.

The SPI interface is a standard SPI interface, shown in the Table 8-1. The SPI interface can be simulated using the general I/O port of the MCU. When the CSN pin is 0, the SPI interface waits for an execution instruction. An instruction is executed once the CSN pin is changed from 1 to 0. The contents of the status register can be read by MISO after the CSN pin changes from 1 to 0.

Table 8-1 SPI interface

PIN	I/O direction	Function description
CSN	Input	SPI Chip Select
SCK	Input	SPI Clock
MOSI	Input	SPI Slave Data Input
MISO	Output	SPI Slave Data Output

8.1 SPI Commands

The SPI commands are shown in Table 8-2.

<Command word: MS Bit to LS Bit (one byte)>

<Data bytes: LS Byte to MS Byte, MS Bit in each byte first>

Table 8-2 SPI commands

Command	Command word (binary)	Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LS Byte first	Read command and status registers. AAAAA =5 bit Register Map Address.
W_REGISTER	001A AAAA	1 to 5 LS Byte first	Write command and status registers. AAAAA = 5 bit Register Map Address. Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32/64 LS Byte first	Read RX-payload. A read operation starts at byte 0. Payload is deleted from RX FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32/64 LS Byte first	Write TX-payload. A write operation starts at byte 0. Used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode.
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode.

REUSE_TX_PL	1110 0011	0	Used for a PTX device, reuse last transmitted payload. TX payload reuse is active until FLUSH_TX is executed. TX payload reuse must be deactivated during package transmission.
ACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: • R_RX_PL_WID • W_TX_PAYLOAD_NOACK • W_ACK_PAYLOAD Using the command again followed by the same data will turn off the above functions. This is executable in power down or standby-I modes only.
DEACTIVATE	0101 0000	1	With this command followed by the data 0x8C, the following functions are turned off: • R_RX_PL_WID • W_TX_PAYLOAD_NOACK • W_ACK_PAYLOAD
R_RX_PL_WID	0110 0000	0	Read the RX FIFO topmost RX-payload data width.
W_ACK_PAYLOAD	1010 1PPP	1 to 32/64 LS Byte first	Used in RX mode. Write PIPE PPP (the value of PPP is from 000 to 101) in response to an ACK while the data is returned. Up to 2 ACK packets can be set. The data of the same PIPE will be sent on a first-in-first-out basis. The write operation usually starts from byte 0.
W_TX_PAYLOAD_NOACK	1011 0000	1 to 32/64 LS Byte first	Write Payload to be transmitted, write operation usually starts from byte 0. Executed in TX mode, use this command to send data, TX_DS flag is given and no auto-answer is awarded after the completion of sending.
CE_FSPI_ON	1111 1101	0	SPI command CE internal logic 1.
CE_FSPI_OFF	1111 1100	0	SPI command CE internal logic 0.
RST_FSPI_HOLD	0101 0011	1	With the command followed by data 0x5A, makes the PAN3020 into reset and maintain.
RST_FSPI_RELS	0101 0011	1	With the command followed by data 0xA5, release the reset and starts to work normally.
REV	1111 1111	0	Read the chip version number: 0X503C

The R_REGISTER and W_REGISTER commands can operate on single or multi-byte registers. When accessing multi-byte registers, first read or write the MS Bit of LS Byte. Terminate the writing before all bytes in a multi-byte register are written, then it leaves the unwritten MS Byte(s) unchanged. For example, the LS Byte of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register. The content of the status register is always read to MISO after a high to low transition on CNS.

8.2 SPI Timing

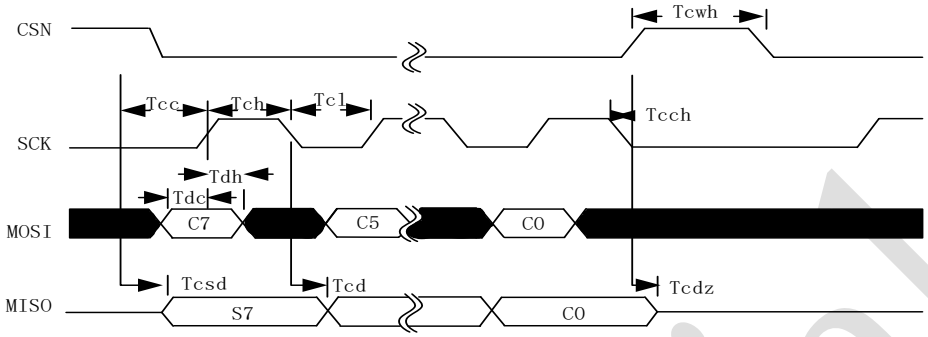

Figure 8-1 SPI NOP timing diagram

Table 8-3 SPI operation reference time

Symbol	Parameters	Min	Max	Units
Tdc	Data set-up time	15	-	ns
Tdh	Data hold time	2	-	ns
Tcsd	CSN signal effective time	-	40	ns
Tcd	SCK signal effective time	-	51	ns
Tcl	SCK signal low-level time	38	-	ns
Tch	SCK signal high-level time	38	-	ns
Fsck	SCK signal frequency	-	8	MHz
Tr,Tf	SCK signal rising/falling time	-	110	ns
Tcc	CSN set-up time	2	-	ns
Tcch	CSN hold time	2	-	ns
Tcwh	CSN invalid time	49	-	ns
Tcdz	CSN signal high impedance	-	40	ns

Note: The parameters of Table 8-3 can be adjusted according to the selected MCU. Be sure to enter sleep mode or standby mode -I before writing registers.

The following symbols are used in the figure:

C_i - SPI instruction bit

S_i – State register bit

D_i – Data bit(Remarks: from low byte to high byte, the high bit in each byte is before)

Among: i=1, 2, 3……n.

8.3 4-wire SPI read operation

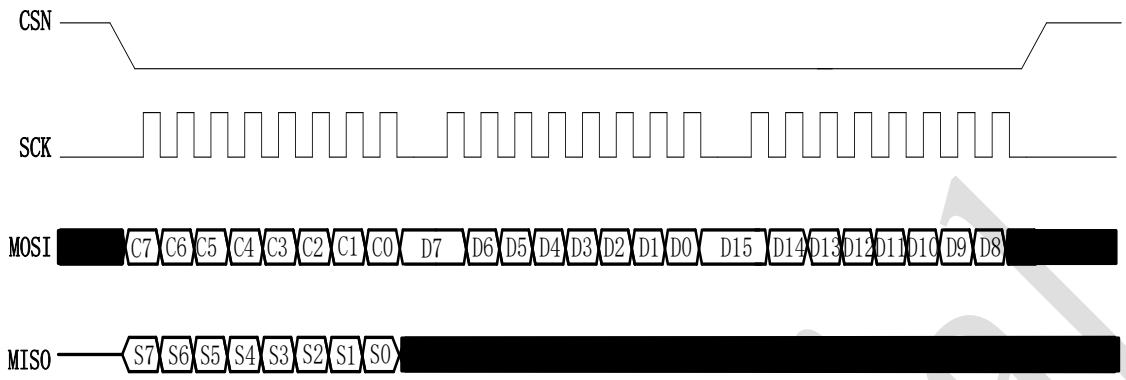

Figure 8-2 4-wire SPI read operation

8.4 4-wire SPI write operation

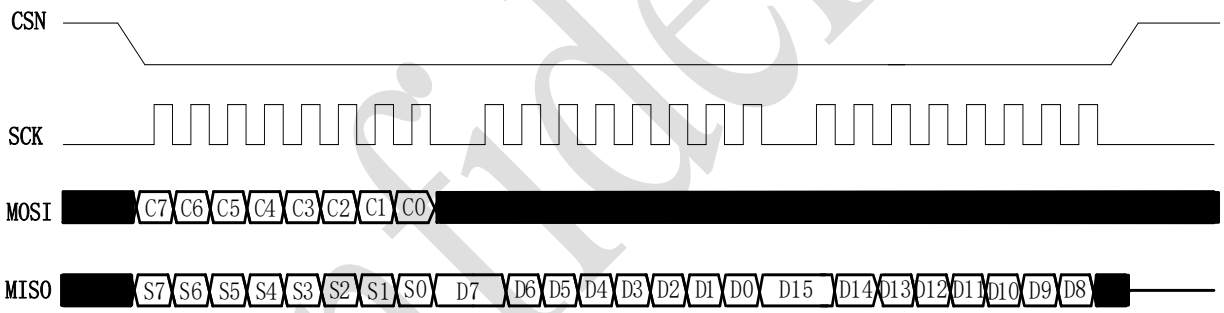

Figure 8-3 4-wire SPI write operation

9 Register Map

The PAN3020 can be configured and controlled by SPI reading/writing the registers shown in the Table 9-1. The undefined register in Table 9-1 reads as "0".

Table 9-1 Register Map

Address（hex）	Register	Bit	Reset value	R/W	Description
00	CONFIG	-	0C	-	Configuration register
	FAST_MODE	7	0	R/W	Fast TX enable 1: Fast TX mode enabled 0: Fast TX mode is not enabled
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR: 1: Interrupt not reflected on the IRQ pin 0: Reflect RX_DR as active low interrupt on the IRQ pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS: 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT: 1: Interrupt not reflected on the IRQ pin 0: Reflect MAX_RT as active low interrupt on the IRQ pin
	EN_CRC	3	1	R/W	CRC enable: 1: CRC enabled 0: CRC is not enabled and CRC calibration is not judged
	CRC_SEL	2	1	R/W	CRC selection 1: CRC16 0: CRC8
	PWR_UP	1	0	R/W	Chip enable: 1: POWER_UP 0: POWER_DOWN
	PRIM_RX	0	0	R/W	RX/TX control: 1: PRX, 0: PTX
01	EN_AA Enhanced Burst	-	01	-	Enable ‘Auto Acknowledgment’ Function
	Reserved	7:6	00	R/W	Only 00 allowed
	ENAA_P5	5	0	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	0	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	0	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	0	R/W	Enable auto acknowledgement data pipe 2

	ENAA_P1	1	0	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0
02	EN_RXADDR	-	01	-	Enabled RX Addresses
	Reserved	7:6	00	R/W	Only 00 allowed
	ERX_P5	5	0	R/W	Enable data pipe 5
	ERX_P4	4	0	R/W	Enable data pipe 4
	ERX_P3	3	0	R/W	Enable data pipe 3
	ERX_P2	2	0	R/W	Enable data pipe 2
	ERX_P1	1	0	R/W	Enable data pipe 1
	ERX_P0	0	1	R/W	Enable data pipe 0
03	SETUP_AW	-	03	-	Setup of Address Widths
	Reserved	7:2	000000	R/W	Only 000000 allowed
	AW	1:0	11	R/W	RX/TX Address field width: '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' – 5 bytes LS Byte is used if address width is below 5
04	SETUP_RETR	-	03	-	Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Retransmit Delay: ‘0000’ – 250μs ‘0001’ – 570μs ‘0010’ – 890μs …….. ‘1111’ – 9530μs Time calculation method: {ARD，7’b1100100}x2.5us
	ARC	3:0	0011	R/W	Auto Retransmit Count: ‘0000’ –Re-Transmit and ACK disabled ‘0001’～‘1111’ – Re-Transmit enabled ‘0001’ – 1 Re-Transmit with ACK ‘0010’ – 2 Re-Transmit with ACK …… ‘1111’ –15 Re-Transmit with ACK
05	RF_CH	-	20	-	RF Channel
	FC8_1	7:0	00100000	R/W	Set the frequency channel decimal places, the 0th bit of FC on RF_ CAL[3]
06	RF_SETUP	-	52	-	RF Setup Register
	RF_DR	7:6	01	R/W	Data Rate 11：400Kbps 10：200Kbps 01：80kbps default 00：40kbps

	FB5_0	5:0	010010	R/W	Set the frequency channel integer bits
07	STATUS	-	-	-	Status Register
	Reserved	7	0	R/W	Only 0 allowed
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO. Write 1 to clear bit.
	TX_DS	5	0	R/W	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit.
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt. write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO: 000-101: Data Pipe Number 110: Not Used 111: RX FIFO Empty
	TX_FULL	0	0	R	TX FIFO full flag: 1: TX FIFO full 0: Available locations in TX FIFO
08	OBSERVE_TX	-	-	-	Transmit observe register
	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH.
	ARC_CNT	3:0	0	R	Count retransmitted packets. Re-Transmit is increased once, ARC_CNT plus one;When the ARC_CNT reaches the ARC limit value, it is considered a packet loss and the PLOS_CNT is added by one; The counter is reset when new data is written to the TX FIFO.
09	DATAOUT	-	-	-	Data Read Registers (for Testing) Select the output according to the DATAOUT_SEL bit, and when the DATAOUT_SEL is 0, read the first test value; When the DATA OUT_SEL is 1, the second test value is read; DATAOUT_SEL defaults to 0.

	ANADATA	7	0	R	analog_data7 or analog_data 3, the default output analog_data7
	ANADATA	6	0	R	analog_data6 or analog_data 2，the default analog_data6s
	ANADATA	5:0	0	R	analog_data [13:8] packet_rssi[5:0] or real_time_rssi[5:0], the default output packet_rssi
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. (LS Byte is written first. Write the number of bytes defined by SETUP_AW).
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LS Byte is written first. Write the number of bytes defined by SETUP_AW).
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2, only the lowest 8 bits. MS Bytes are equal to RX_ADDR_P1[39:8].
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3, only the lowest 8 bits. MS Bytes are equal to RX_ADDR_P1[39:8].
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4, only the lowest 8 bits. MS Bytes are equal to RX_ADDR_P1[39:8].
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5, only the lowest 8 bits. MS Bytes are equal to RX_ADDR_P1[39:8].
10	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	Transmit address. (LS Byte is written first) Used for a PTX device only. Set RX_ADDR_P0 equal to the address in order to receive ACK autorespondence.
11	RX_PW_P0	-	00	-	Number of bytes in RX payload in data pipe 0
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P0	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 0 (1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
12	RX_PW_P1	-	00	-	Number of bytes in RX payload in data pipe 1

	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P1	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 1 (1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
13	RX_PW_P2	-	00	-	Number of bytes in RX payload in data pipe 2
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P2	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 2 (1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
14	RX_PW_P3	-	00	-	Number of bytes in RX payload in data pipe 3
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P3	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 3 (1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
15	RX_PW_P4	-	00	-	Number of bytes in RX payload in data pipe 4
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P4	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 4(1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
16	RX_PW_P5	-	00	-	Number of bytes in RX payload in data pipe 5
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P5	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 5 (1 to 64 bytes).

					0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
17	FIFO_STATUS	-	-	-	FIFO Status Register and analog_ data[5:4]/[1:0]
	reserved	7	0	R	N/A
	TX_REUSE	6	0	R	Invokes the indicator bits sent by the previous frame of data. After using the REUSE_TX_PL command, the bit is 1, retransmitting the last frame of data from the previous transmission. This bit can be reset by commands W_TX_PAYLOAD, W_TX_PAYLOAD_NOACK, DEACTIVATE, FLUSH TX.
	TX_FULL	5	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
	TX_EMPTY	4	1	R	TX FIFO empty flag: 1: TX FIFO empty 0: Data in TX FIFO
	ANADATA	3	0	R	analog_data[4] or analog_data[1], selected by the DATAOUT_SEL, the default output analog_data4
	ANADATA	2	0	R	analog_data[5] or analog_data[0], selected by the DATAOUT_SEL, the default output analog_data5
	RX_FULL	1	0	R	RX FIFO full flag: 1: RX FIFO full 0: Available locations in RX FIFO
	RX_EMPTY	0	1	R	RX FIFO empty flag: 1: RX FIFO empty 0: Data in RX FIFO
N/A	TX_PLD	255:0	X	W	TX sends data TX data is written via SPI commands, which are stored in a Level 2 32-byte or Level 1 64-byte FIFO
N/A	RX_PLD	255:0	X	R	RX receives data RX data is read out via SPI command, which is stored in a Level 2 32-byte or Level 1 64-byte FIFO, all of the RX PIPE share the same

					FIFO
18	RF_CAL3	39:0	9602A81000	-	Supplement RF registers (Generally use the default value)
	VCO_SWC	39:37	100	R/W	PLL VCO BANK capacitor setting 111: Multi-capacitance 000: Less capacitance
	EN_VCO_CAL	36	1	R/W	PLL VCO auto-correction enable bit 1: Enable 0: Not enabled
	GAUSS_CTRL	35:34	01	R/W	TX mode setting High. 1: Fractional TX 0: Two-point TX Low. 1: Output to DAC with one beat delay 0: Output to DAC without delay
	CLK_EN	33	1	R/W	PLL DELTA-SIGMA modulator clock enable setting 1: Enable 0: not enabled
	CTL_DITHER_LSB	32:30	000	R/W	PLL DELTA-SIGMA modulator DITHER factor setting 111: Factor 7 000: Factor 0
	CTL_DITHER_SHAPE	29	0	R/W	PLL DELTA-SIGMA modulator DITHER module enable setting 1: Enable 0: Not enabled
	DIV2_EN	28	0	R/W	PLL DELTA-SIGMA modulator DIV2 module enable setting 1: Enable 0: Not enabled
	DS_SHIFT	27	0	R/W	PLL DELTA-SIGMA modulator shift enable setting 1: Enable 0: No enable
	SPI_DAC_TEST	26	0	R/W	TX DAC output test enable setting 1: Enable 0: Not enabled
	IBDIV_SEL	25:24	10	R/W	PLL divider bias current setting: 11: High current 10: Small current
	IBH_SEL	23:22	10	R/W	PLL divide-by-2 divider bias current setting:

					11: High current 10: Small current
	IBL_SEL	21:20	10	R/W	PLL divide-by-4/6 divider bias current setting: 11: High current 10: Small current
	IBPRE_SEL	19:18	10	R/W	PLL divide-by-8/9 divider bias current setting: 11: High current 10: Small current
	INV_CLK_EN	17	0	R/W	PLL DELTA-SIGMA modulator inverse operating mode enable setting 1: Enable 0: Not enabled
	N/A	16	0	R/W	N/A
	MASH2_MODE	15	0	R/W	PLL DELTA-SIGMA modulator mash2 mode enable setting 1: Enable 0: Not enabled
	POLAR	14	0	R/W	PLL VCO polarity setting 1: Negative polarity 0: Positive polarity
	SHIFT_OFFSET	13	0	R/W	PLL DELTA-SIGMA modulator shift bias enable setting 1: Enable 0: Not enabled
	SPI_CAL_TRIG	12	1	R/W	PLL VCO auto-correct SPI trigger level setting with edge trigger mode (both rising and falling edges) 1: High level 0: Low level
	CAL_VREF_SEL	11	0	R/W	PLL VCO Auto-Correct reference voltage Setting 1: Low voltage 0: High voltage
	TST_BPF	10	0	R/W	Filter signal output to PIN 1: Enable 0: Not enabled
	MCU_CLK_EN	9	0	R/W	Enable signal sent to MCU clock 1: Enable 0: No enable
	TP_CODE_OFFSET	8:6	000	R/W	Two-point calibration offset (signed numbers)

					000: 0 100: -4 011: 3 111: -1
	CP_SEL	5:4	00	R/W	PLL charge pump current setting 00: 26uA 01: 52uA 10: 78uA 11: 104uA
	TST_EN	3	0	R/W	Enter the test mode enable setting 1: Enable 0: Not enabled
	LPF_RES_SEL0P	2	0	R/W	PLL filter stage setting 1: Two stages 0: Three stages
	LPF_RES_SEL1P	1	0	R/W	PLL filter three-stage pole setting 1: High pole 0: Low pole
	DA_LPF_BW	0	0	R/W	TX DAC filter bandwidth setting 1: Bandwidth 2MHz 0: Bandwidth 1MHz
19	DEMOD_CAL	39:0	8B7449DC01	-	Modulation and demodulation parameter register (configurable by program needs)
	GAUSS_SCALE	39:36	1000	R/W	The signal size adjustment of the Gaussian filter output to Delta-Sigma, which is one of the determining factors for the size of the transmit modulation frequency offset 1111: Smaller signal .... 1000: Medium signal .... 0000: Larger signal
	F_SEL	35:34	10	R/W	TX modulation frequency offset setting 11: Small frequency offset 00: Large frequency offset
	F_SEL_1	33:27	1101110	R/W	TX modulation frequency offset setting 0000000: Small frequency offset ..... 1111111: Large frequency offset
	GAUSS_SCALE_1	26:23	1000	R/W	The signal size adjustment of the Gaussian filter 1 output to DAC, which is one of the

					determining factors for the size of the transmit modulation frequency offset 1111: Smaller signal .... 1000: Medium signal .... 0000: Larger signal
	DA_VREF_MB	22:20	100	R/W	The high reference voltage bit of DAC. Larger value of high reference voltage bit, larger DAC output amplitude 111: High reference voltage bit value is large 000: High reference voltage bit value is small
	DA_VREF_LB	19:17	100	R/W	The low reference voltage bit of DAC. Smaller value of low reference voltage bit, larger DAC output amplitude 111: low reference voltage bit value is small 000: Low reference voltage bit value is large
	SEL_SW	16:14	111	R/W	DAC output amplitude selection 111: High amplitude 000: Low amplitude
	VCO_CODE_IN	13:10	0111	R/W	VCO band selection bit, which is only valid when the EN_VCO_CAL is 0 1111: High band 0000: Low band
	TX_2M	9	0	R/W	VCO offset setting (for large frequency offsets) 11: High frequency offset 00: Low frequency offset
	TX_0P5M	8	0	R/W	VCO offset setting (for small frequency offsets) 11: High frequency offset 00: Low frequency offset
	CHIP_CARR	7:5	0	R/W	Set whether the chip enters carrier test mode 111: Enter single carrier test mode 000: Exit single carrier test mode
	INT_MODE_EN	4	0	R/W	PLL operating mode setting 1: Integer mode 0: Decimal mode
	SPI_CPO	3	0	R/W	PLL charge pump test output enable 1: Enable 0: Not enabled
	SPI_VCTRL	2	0	R/W	PLL Vctrl test enable 1: Enable

					0: No enable
	SPI_LPF_SEL	1	0	R/W	PLL loop filter setting 0: Chip internal filter 1: Chip external filter
	SCR_EN	0	1	R/W	Whether the scrambling function is enabled or not, the scrambling function can be enabled to whiten the data to be sent, thus reducing the long 1 and long 0 data. Enable the scrambling function requires the same configuration for both the transmitter and receiver 1: Enable scrambling 0: Disable scrambling
1A	RF_CAL2	39:0	F608DDFECB	-	Supplementary RF register (generally use default values)
	CTL_FRE	39:34	111101	R/W	Crystal capacitor array setting 111111: More capacitance 000000: Less capacitance
	CLKOUT_Z_sel	33	1	R/W	Whether the CLKOUT pin is a high-impedance output 1: CLKOUT PIN is a high-impedance output 0: CLKOUT PIN as Output
	CE_L_sel	32	0	R/W	CE pin weak pull-down resistor enable or not 1: CE pin weak pull-down resistor is enabled 0: CE pin weak pull-down resistor is not enabled
	MISO_Z_sel	31	0	R/W	Whether the MISO pin is a high-resistance output 1: MISO PIN as high resistance output 0: MISO PIN as Output
	IRQ_Z_SEL	30	0	R/W	Whether the IRQ pin is a high-resistance output 1: IRQ PIN as high resistance output 0: IRQ PIN as Output
	SYNC_BYPASS	29:28	00	R/W	Controls whether dig2's synchronizer by_pass 1: bypass, 0: no bypass High controls gauss_filter Low control gauss_filter_1
	CLK_SEL	27:26	10	R/W	Internal crystal signal output frequency selection 00: 16MHz

					01: 8MHz 10: 4MHz 11: 2MHz
	ADJ1	25	0	R/W	Receive POLYPHASE filter path setting 1: By Buffer 0: Not by Buffer
	ADJ3	24	1	R/W	Receive POLYPHASE filter path setting 1: By Buffer 0: Not by Buffer
	TEMP_GAIN	23:22	01	R/W	Temperature sensing circuit output voltage gain adjustment 11: The output gain is large 00: The output gain is small
	LIM_SEL	21	0	R/W	Limter level setting 1: Two levels 0: Seven levels
	MIXL_BC	20	1	R/W	Receive MIXL current setting 1: ×1 0: ×0.5
	IFBUF_GC	19:18	11	R/W	Receive IFBUF gain setting 11: High gain 00: Low gain
	IQS	17	0	R/W	Receive POLYPHASE filter IQ switching setting 1: I-way 0: Q-way
	PA1_CTM	16:15	11	R/W	TX driver stage PA resonant capacitor setting 11: More capacitance 00: Less capacitance
	PA2_CTM	14:13	11	R/W	TX output stage PA resonant capacitor setting 11: More capacitance 00: Less capacitance
	EN_BUF	12	1	R/W	Receive filter buffer enable setting 1：Enable 0：No enable
	I_SEL	11	1	R/W	TX F2S module I enable setting 1: Enable 0: Not enabled
	Q_SEL	10	1	R/W	TX F2S module Q enable setting 1: Enable 0: Not enabled

	RES_SEL	9:8	10	R/W	Power management reference resistor setting 11: 20k 10: 22k 01: 24k 00: 26k
	PD_ADC	7	1	R/W	Receive the ADC enable setting in RSSI 1: Not enabled 0: Enable
	GC_SK	6	1	R/W	Receive SallenKey filter (before SC) gain control 1: High gain 0: Low gain
	IB_BPF_SC	5:4	00	R/W	SC filter current control bit 11：SC filter current is larger 00：SC filter current is small
	IB_BPF_SK	3:2	10	R/W	SK filter current control bit 11：SK filter current is larger 00：SK filter current is small
	TST_ADC	1	1	R/W	1 ） TST_ADC= 0, TST_RSSI=1, and TST_EN=1, PIN AIO is used as the ADC analog input to test the supply voltage or temperature sensor voltage signal; 2) TST_ADC= 0, TST_RSSI=1, and TST_TEMP=0, TEMP module output to ADC, PIN AIO as TEMP signal analog output, test temperature-sensitive voltage; 3）TST_ADC= 1, TST_RSSI=0, PIN AIO is used as the analog output of RSSI signal 4) TST_ADC= 1, TST_RSSI=1, PIN AIO is not used as the input and output, is the normal operation mode of RSSI signal sent to the ADC.
	TST_RSSI	0	1	R/W	
1B	DEM_CAL2	31:0	0400E70B	-	Supplementary demodulation parameter register (Generally use the default value)
	RESERVED	31:28	0000	R/W	N/A
	IRQ_inv_sel	27	0	R/W	IRQ/EN_P reverse output control 0: No reverse output 1: Direction output
	EN_STBII_TXRX	26	1	R/W	Enhanced mode, insert a STB2 state TX/RX in the middle of TX to RX 1: Enable, 0: Not enabled
	DATAOUT_SEL	25	0	R/W	Data read selection bit (for testing)

					1: The value read by the 0X09 DATAOUT register is the value of the first test function 0: The value read by the 0X09 DATAOUT register is the value of the second test function
	FEC_EN	24	0	R/W	FEC function enables signal 1: Enable 0: Not enabled
	PIN_MODE	23:21	000	R/W	Set the output PIN (MISO pin/IRQ pin) when the chip enters the test mode 000 (and CHIP is 0) is the operating mode, for data output and interrupt output 000 (and CHIP is 1) is test sensitivity mode, for demodulation data and clock output 110 (and CHIP is 1) is the test receive mode, for limit I and Q outputs
	EN_RX_MODE	20	0	R/W	Whether the receive channel is opened at the same time as the PLL 1: Open at the same time 0: Open in time share
	DELAY1	19	0	R/W	demod_test <= delay1;
	en_two_point_cal	18	0	R/W	Two-point auto-calibration enable setting 1: Enable 0: Not enabled
	two_point_spi_trig	17	0	R/W	Two-point auto-calibration trigger setting: 1: Not enabled 0: Enable
	PTH	16:13	0111	R/W	Receiver digital demodulator preamble correlation threshold setting, 24-bit preamble correlation threshold = PTH+16 1000: 24 bits 0110: 22 bits 0000: 16 bits
	SYNC_SEL	12	0	R/W	The receiver digital demodulator samples 4 times, and takes a few points related to calculate the bit data correctly 1: 3bit 0: 2bit
	DECOD_INV	11	0	R/W	Whether the preamble is negated bitwise, generally set to 1 Enabling this function requires both sides of the transceiver 1: Do not negate bitwise

					0: Bitwise negation
	GAIN1	10:7	1110	R/W	The demodulator's data center value adjusts the amplitude of the reference waveform of the loop to 1110
	GAIN2	6:1	000101	R/W	The adjustment speed of the demodulator's data center value adjustment loop according to the reference waveform is set to 000101.
	AGGRESSIVE	0	1	R/W	Speed selection of the demodulator's bitrate synchronization unit 1: Large step adjustment, fast speed 0: Small step adjustment, slow speed
1C	DYNPD	-	00	-	Dynamic PAYLOAD length enable
	Reserved	7:6	00	R/W	Only 00 allowed
	DPL_P5	5	0	R/W	Enable PIPE 5 dynamic PAYLOAD length (requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable PIPE 4 dynamic PAYLOAD length (requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable PIPE 3 dynamic PAYLOAD length (requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable PIPE 2 dynamic PAYLOAD length (requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable PIPE 1 dynamic PAYLOAD length (requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable PIPE 0 dynamic PAYLOAD length (requires EN_DPL and ENAA_P0)
1D	FEATURE	7:0	00	R/W	Feature Register
	Reserved	7	0	R/W	Only 00 allowed
	MUX_PA_IRQ	6	0	R/W	Select IRQ signal output or EN_PA signal output to PIN 0: IRQ signal output to PIN 1: EN_PA signal output to PIN
	CE_SEL	5	0	R/W	Enable CE to be enabled by command 0: CE is controlled by CE PIN 1: CE is controlled by command
	DATA_LEN_SEL	4:3	00	R/W	Data length selection 11: 64byte (512bit) mode 00: 32byte (256bit) mode
	EN_DPL	2	0	R/W	Enables dynamic PAYLOAD length
	EN_ACK_PAY	1	0	R/W	Enable ACK with payload
	EN_NO_ACK	0	0	R/W	Enable W_TX_PAYLOAD_NOACK command
1E	RF_CAL	39:0	48DFFDFB10	R/W	RF parameter register (configurable by program needs)

	RESERVED	39	1	R/W	N/A
	RSSI_RES	38:37	10	R/W	Signal gain selection bit for RSSI 00: Minimum gain 11: Maximum gain
	PD_RSSI	36	0	R/W	RSSI function enable 1: Enable 0: Not enabled
	GC_BUF	35:34	10	R/W	Filter module 3 gain setting 10: High gain 01: Low gain
	CTL_BW	33:31	001	R/W	Filter bandwidth control: 40kbps：000； 80kbps：001； 200kbps：011； 400kbps：111；
	MIXL_GC_CTR	30	1	R/W	MIX gain setting 1: High gain 0: Low gain
	LO_PH_BC	29	0	R/W	LO driver current selection 1: Low current 0: High current
	LNA_BC	28:27	11	R/W	LNA current setting 11: High current 00: Low current
	LNA_GC	26:25	11	R/W	LNA gain selection 11: Maximum gain 00: Minimum gain
	PA2_LVL	24:19	111111	R/W	TX output stage PA output amplitude setting 11111: Maximum amplitude output 00000: Minimum amplitude output
	PA2_BC	18:17	10	R/W	TX output stage PA current setting 11: High current 00: Low current
	PA1_LVL	16:11	111111	R/W	TX drive stage PA output amplitude setting 111111: Maximum amplitude output 000000：Minimum amplitude output
	PA1_BC	10:9	01	R/W	TX drive stage PA current setting 11: High current 00: Low current
	VCO_IB	8:6	100	R/W	PLL VCO current setting 111: High current 000: Low current

	HI_LO_SET	5	0	R/W	Receive high and low Local Oscillator settings 1: High LO 0: Low LO
	HS_SEL	4	1	R/W	PLL divide by 2 output setting HS_SEL LS_SEL=10: High frequency output HS_SEL LS_SEL=01: Low frequency output
	FC_0	3	0	R/W	FC lowest
	LS_SEL	2	0	R/W	PLL divide by 4 or divide by 6 output setting 0: Divide by 4 1: Divide by 6
	TST_TEMP	1	0	R/W	The temperature-sensitive module enable setting 0: Enable 1: Not enabled
	HL_SEL	0	0	R/W	PLL divide by 2 or divide by 3 setting 0: Divide by 2 1: Divide by 3
1F	BB_CAL	39:0	041F671C09	R/W	Digital baseband parameter register (Generally use the default value)
	CE_JUST_TIME	39:33	0000010	R/W	The default is 10us, and if you do not want to modify the pth of PRX in fast_mode, you can appropriately increase the CE_JUST_ TIME of PTX, the length of time can be calculated as the following formula: CE_JUST_TIME × 5, the unit is us Minimum value: 0us Maximum value: 635us
	ldo_src	32	0	R/W	1 : LDO_EN control line shield LDO operation in STB2 state; 0 : LDO_EN control line LDO characteristics in STB2 state are subject to state machine operation.
	INVERTER	31	0	R/W	Whether to reverse the RX path data before entering RX Block: 1: reverse 0: remain unchanged
	Reserved	30	0	R/W	N/A
	DAC_BASAL	29:24	011111	R/W	The initial offset of DAC input.
	TRX_TIME	23:21	011	R/W	The time from PLL Open to sending data packet, the length of time can be calculated

					as the following formula: TRX_TIME × 10 + 2.5, the unit is us. Default 32.5us, 2.5us~72.5us
	EX_PA_TIME	20:16	00111	R/W	The time from TX PLL enable to PA enable, the length of time can be calculated as the following formula: EX_PA_TIMEx20, the unit is us. Default 140us, 0us~620us
	TX_SETUP_TIME	15:11	00011	R/W	The time from PA enable to TX PLL Open, the length of time can be calculated as the following formula: TX_SETUP_TIME×20, the unit is us. Default 60us, 0us~620us
	RX_SETUP_TIME	10:6	10000	R/W	RX RF path PLL stabilization time, the length of time can be calculated as the following formula: RX_SETUP_TIME×20, the unit is us. Default 320us, 0us~620us
	RX_ACK_TIME	5:0	001001	R/W	The maximum time to wait for ACK after the PTX turns to RX mode, beyond which the transmission is considered to have failed: For 400Kbps data rata, the length of time can be calculated as the following formula: RX_ACK_TIME×40+37us, default 397us, 37us~2557us. For 200Kbps data rata, the length of time can be calculated as the following formula: RX_ACK_TIME×80+77us, default 797us, 77us~5117us. For 80Kbps data rata, the length of time can be calculated as the following formula: RX_ACK_TIME×160+157, default 1597us, 157us~10237us. For 40Kbps data rata, the length of time can be calculated as the following formula: RX_ACK_TIME×320+317, default 3197us, 317us~20477us.

Notes:

- The initial values for all registers (including read/write) after power-on reset on the PAN3020 are described in the table.
- When accessing multibyte registers/addresses/data, the read/write order is low byte before high byte after. Single byte internal high bit is before low bit is after.

10 Application Reference Design

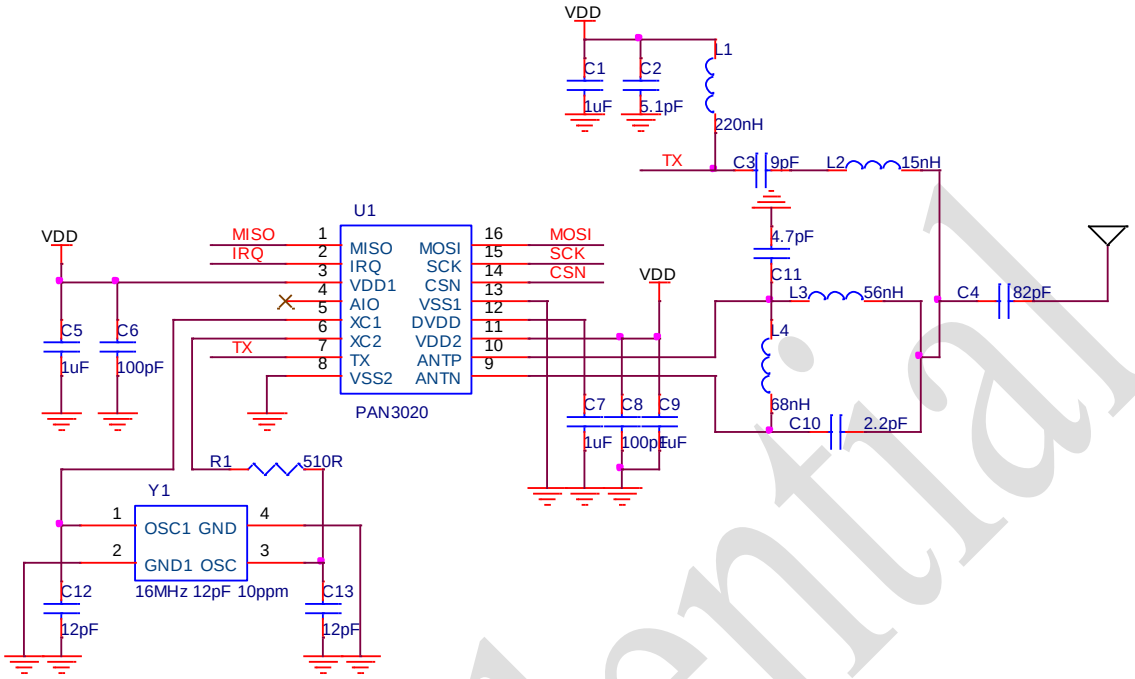

Figure 10-1 433MHz band application circuit for SOP16 package

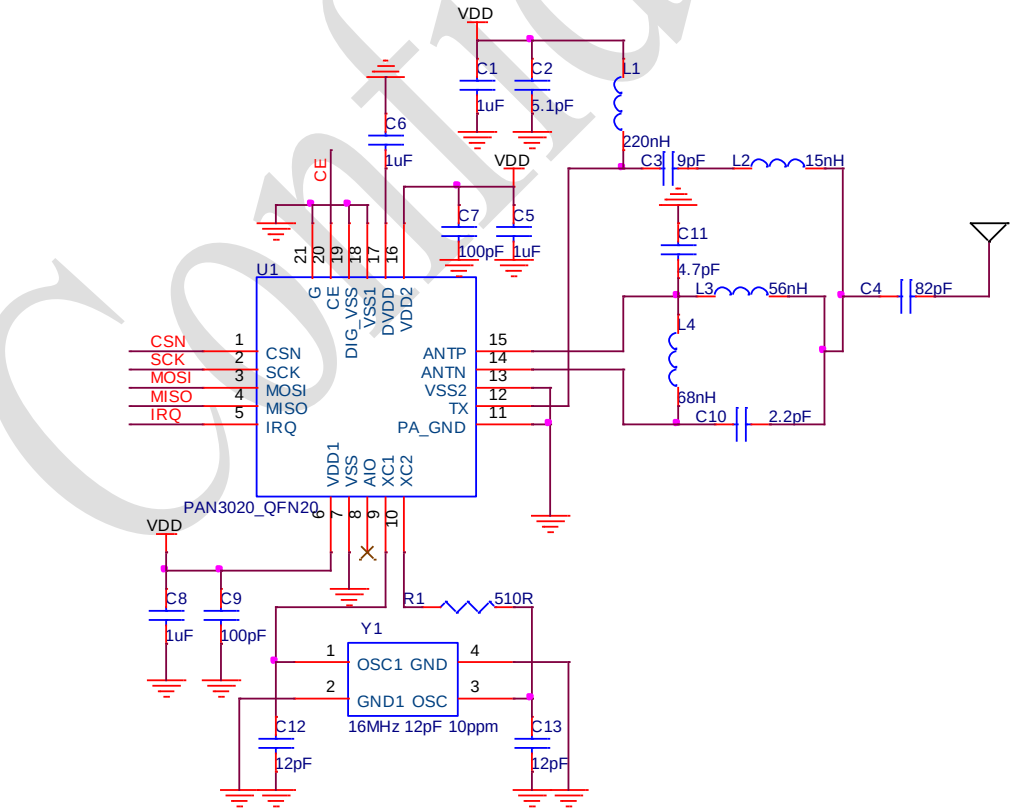

Figure 10-2 433MHz band application circuit for QFN20 package

The corresponding matching relationship of each frequency band is shown in Table 10-1.

Table 10-1 Matching table for each frequency band

Band（MHz）	L1(nH)	C3(pF)	L2(nH)	L3(nH)	L4(nH)	C10(pF)	C11(pF)
315	220	12	22	68	120	2.2	6
433	220	9	15	56	68	2.2	4.7
868	100	3.3	6	24	27	1	3.6
915	100	3	6	22	22	1	3.6

Table 10-2 Recommended crystal matching parameters

Crystal load capacitance	External matching capacitor
12 pf	12 pf
20 pf	20 pf

11 Package Dimensions

11.1 SOP16 package

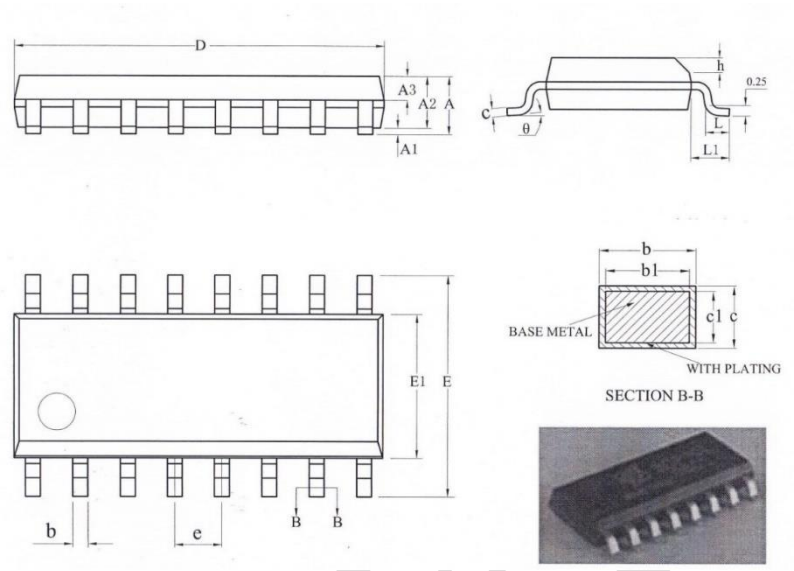

Figure 11-1 Package diagram for the SOP16 package

Table 11-1 Package detail parameters for the SOP16 package

SYMBOL	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
Ø	0	-	8°

Note: Units of measure is millimeter.

11.2 QFN20 package

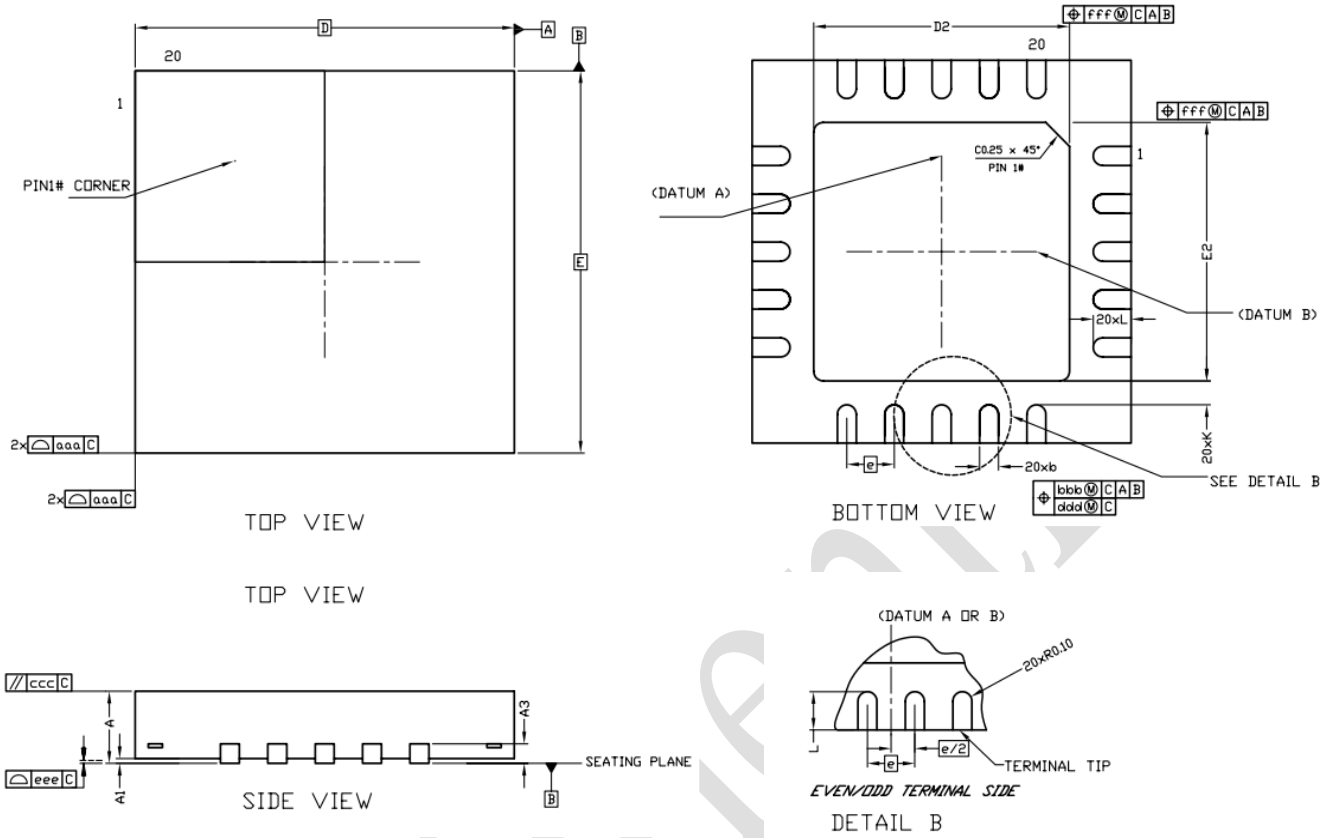

Figure 11-2 Package diagram for the QFN20 package

Table 11-2 Package detail parameters for the QFN20 package

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.85	0.90	0.95
A1	0	0.02	0.05
A3	-	0.20REF	-
b	0.15	0.20	0.25
D	4.00BSC		
E	4.00BSC		
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.50BSC		
L	0.35	0.40	0.45
K	0.20	-	-
aaa	0.10		
bbb	0.07		
ccc	0.10		

ddd	0.05
eee	0.08
fff	0.10

Note: Units of measure is millimeter.

12 Precautions

1) This product is a CMOS device and should be protected against static electricity during storage, transportation and use.
2) Grounding when device is in use.
3) Reflow temperature can not exceed 260℃.

   The lead-free reflow soldering process is shown in the figure below:

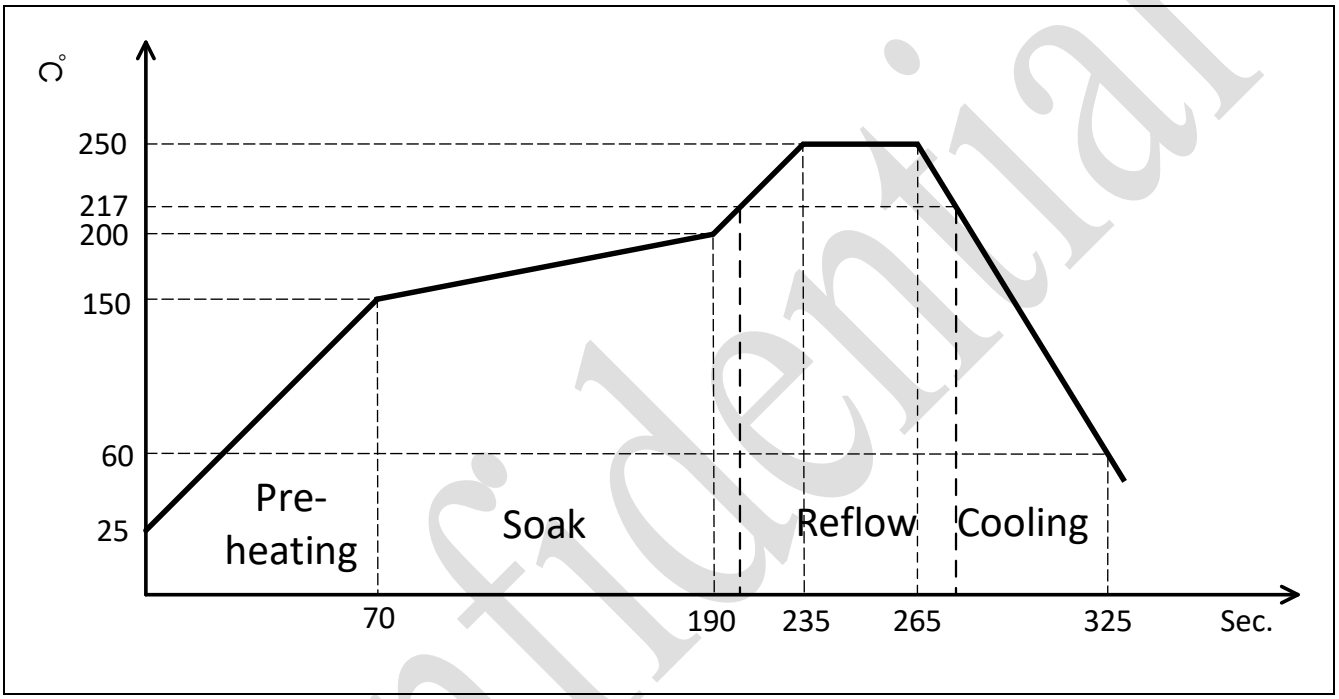

Figure 12-1 Reflow Profile

13 Storage Conditions

1) Products should be stored in sealed packages: when the temperature is less than 30 degrees and the humidity is less than 90%, it can last for 12 months.
2) After the package is opened, the components will be used in the reflow process or other high-temperature processes. The following conditions must be met:
   a) Completed within 72 hours and the factory environment is less than 30℃≤ 60% RH.
   b) Stored in 10% RH environment.
   c) Exhaust at 125℃ for 24 hours to remove internal water vapor before used.
3) MSL (Moisture Sensitivity Level): Level-3 (based on IPC/JEDEC J-STD-020)