Panchip Microelectronics Co., Ltd.

PAN3028

Datasheet brief

Low Power, Long Range, Sub-1GHz RF Transceiver

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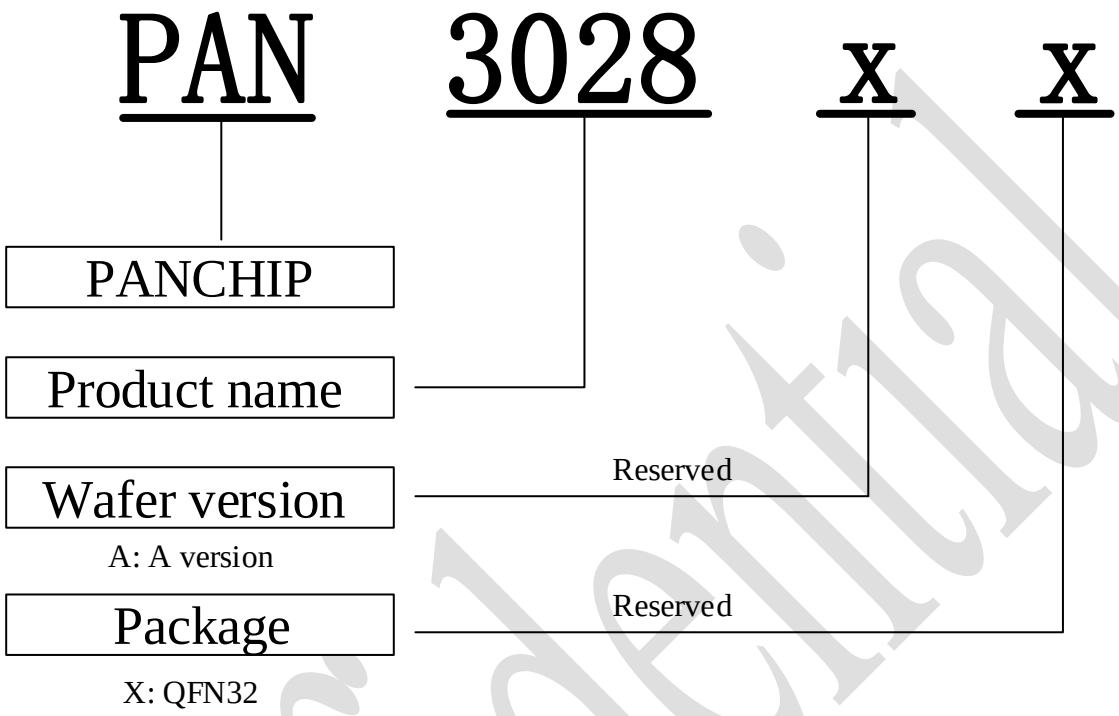
REVISION HISTORY

Version	Date	Content
V1.1	2019.06	Initial
V1.2	2019.07	Addition of Interface description and Electrical Characteristics
V1.3	2019.11	Change the package form to QFN28
V1.4	2020.06	Change the package form to QFN32
V1.5	2020.07	Addition of Pin 33
V1.6	2021.04	● The operating frequency band is expanded to 370~600 MHz and 740~1200MHz ● Increase the maximum link budget to 162dB ● Increase the maximum transmission power to 22dBm ● Current consumption at the maximum transmission power: 135mA@22dBm
V1.7	2021.10	● Addition of Naming Rules and Product Series ● Update Application Reference Diagram and related parameter descriptions
V1.8	2022.02	● The operating frequency band is modified to 370~590MHz and 740~1180MHz ● Addition of a note under section 5.3 RF Performance Table
V1.9	2022.06	Update Application Reference Diagram
V2.0	2023.05	Added the packing information and reflow profile
V2.1	2023.10	Updated the transmit output power

Naming Rules



Ordering Information

Product series	Wafer version	Pack-age	GPIO	Deep Sleep mode current	Transmit output power	Temperature	Packing
PAN3028AX	A	QFN32	6	400nA	-23.5 ~ 22dBm	-40 ~ 85℃	Tape & Reel

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Abbreviation

ADC	Analog-to-Digital Converter
CAD	Channel Activity Detection
CSN	SPI chip select signal
DAC	Digital-to-Analog Converter
DCDC	DC converter
FIFO	First Input First Output
GPIO	General-purpose I/O
IRQ	Interrupt ReQuest
LDO	Low Dropout Regulator
LPF	Low Pass Filter
MAC	Media Access Control Layer
MCU	Microcontroller Unit
OSC	Oscillator
PA	Power Amplifier
RF	Radio Frequency
PLL	Phase Locked Loop
PMU	Power Management Unit
POR	Power-on reset
RAM	Random Access Memory
SCK	SPI Serial Clock
SF	Spreading Factor
SPI	Serial Peripheral Interface
STB	Standby Mode
Sync	Synchronize
VCO	Voltage Controlled Oscillator

1 General Description

PAN3028 is a low-power long-range wireless transceiver chip using ChirpIoT™ modulation and demodulation technology. It supports half-duplex wireless communication. The operating frequency band is 370~590MHz and 740~1180MHz. The chip has the characteristics such as high anti-interference, high sensitivity, low power consumption and ultra-long transmission range. The industry-leading link budget, along with the -140dBm sensitivity and the 22dBm maximum output power makes this chip the best choise for long-range transmission and extremely high reliability applications.

Compared with conventional modulation techniques, PAN3028 also has significant advantages in blocking and adjacent channel selection, which further improves communication reliability. A lot of chip parameters, such as bandwidth, spreading factor, coding rate of forward error correction, can be configured for trade-off among distance, anti-interference ability and power consumption, which ensures sufficient flexibility.

1.1 Key Features

- Frequency band: 370~590 MHz, 740~1180MHz
- Modulation: ChirpIoT™
- Transmitter output power: -23.5dBm ~ 22dBm
- Max link budget: 162dB
- Sensitivity: -140dBm@62.5KHz
- Operating current
  - Deep Sleep mode current: 400nA
  - Receiving current: 12.5mA@DCDC mode
  - Transmitting current: 135mA@22dBm, 83mA@18dBm, 25mA@0dBm
- Bandwidth: 62.5KHz, 125KHz, 250KHz, 500KHz
- Spreading Factor (SF): 7~12, supports automatic identification of spread factors
- Coding Rate (CR): 4/5, 4/6, 4/7, 4/8
- Supports CAD function
- Data rate: 0.08~20.4Kbps
- Supports 4-wire SPI configuration interface and 6 GPIOs
- Fully integrated frequency synthesizer
- Operating voltage range: 1.8V ~3.6V, 2V~3.6V in DCDC mode
- Operating Temperature: -40℃~85℃
- Package: QFN32, 5×5mm

1.2 Typical Applications

- Smart industry
- Smart agriculture
- Smart community
- Smart meter
- Smart healthcare
- Smart firefighting

2 Block Diagram

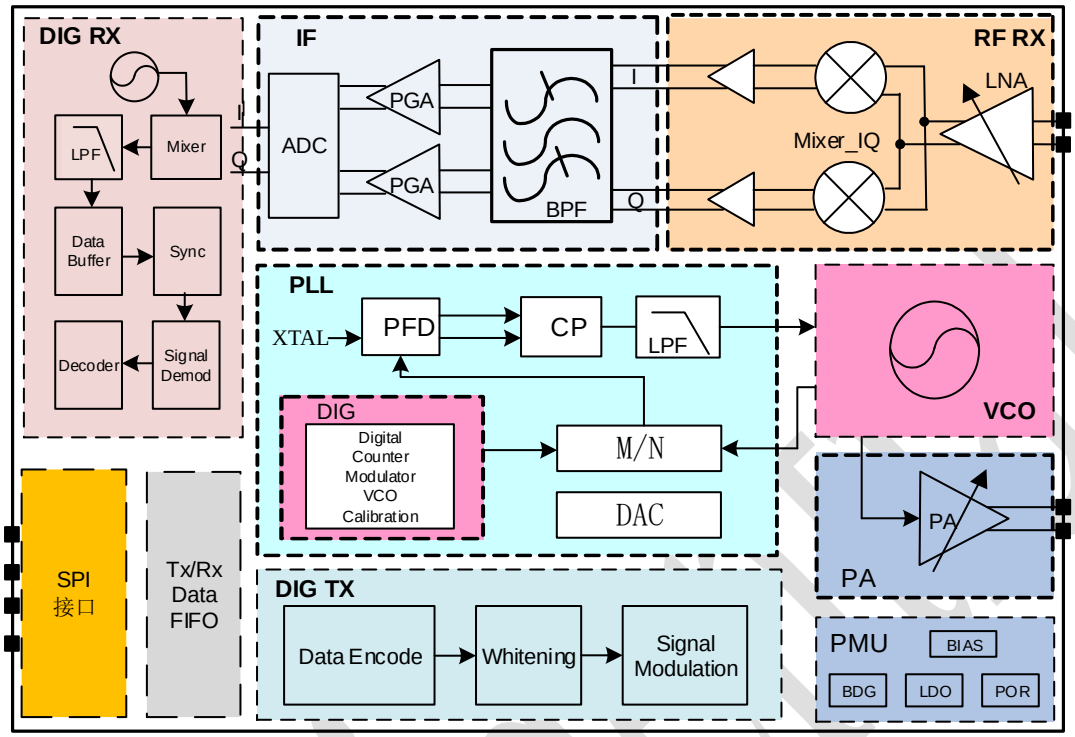

Figure 2-1 PAN3028 Block Diagram

3 Pin Information

3.1 Pin Diagram

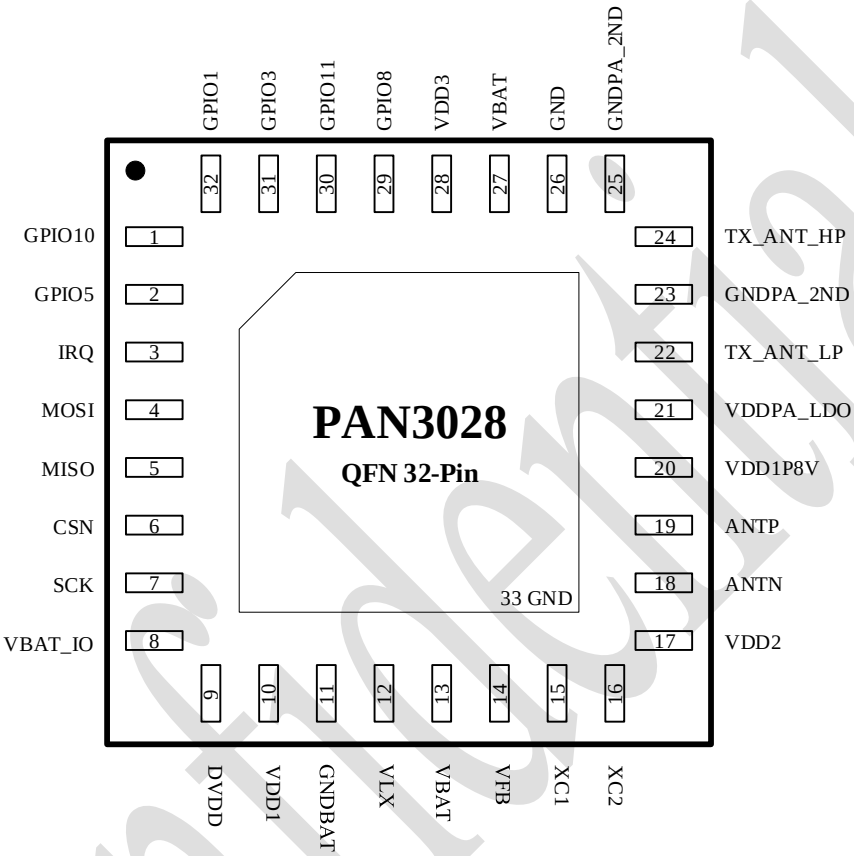

Figure 3-1 PAN3028 pin diagram

3.2 Pin Descriptions

Table 3-1 PAN3028 pin descriptions

Pin No.	Pin Name	Pin Type	Description
1	GPIO10	I	Digital input Pin
		O	External PA enable control signal
2	GPIO5	I/O	Digital I/O Pin, software configurable
3	IRQ	O	Interrupt signal
4	MOSI	I	SPI slave input
5	MISO	O	SPI slave output
6	CSN	I	SPI Chip Select
7	SCK	I	SPI clock

8	VBAT_IO	P	Digital GPIO power supply, connected to the main power supply
9	DVDD	P	Digital power LDO output
10	VDD1	P	Analog power supply, connected to VFB in DCDC mode, connected to the main power supply in non-DCDC mode
11	GNDBAT	G	Analog ground
12	VLX	AO	Internal DCDC output, connected to external series inductor in DCDC mode, NC in non-DCDC mode
13	VBAT	P	Analog power supply, connected to the main power supply
14	VFB	AI	Internal DCDC feedback input, connected to VDD in DCDC mode, NC in non-DCDC mode
15	XC1	AI	Crystal oscillator input
16	XC2	AO	Crystal oscillator output
17	VDD2	P	Analog power supply, connected to VFB in DCDC mode, connected to the main power supply in non-DCDC mode
18	ANTN	AI	Antenna Pin（Negative）
19	ANTP	AI	Antenna Pin（Positive）
20	VDD1P8V	P	Low power PA LDO power supply, connected to VFB in DCDC mode, connected to the main power supply in non-DCDC mode
21	VDDPA_LDO	P	Low power LDO output
22	TX_ANT_LP	AO	Transmitter low power PA output
23	GNDPA_2ND	G	Analog ground
24	TX_ANT_HP	AO	Transmitter high power PA output
25	GNDPA_2ND	G	Analog ground
26	GND	G	Ground Pin
27	VBAT	P	Analog power supply, connect to the main power supply
28	VDD3	P	Analog power supply, connected to VFB in DCDC mode, connected to the main power supply in non-DCDC mode
29	GPIO8	I/O	Digital I/O Pin
30	GPIO11	I	Digital I/O Pin
		O	Channel status indication signal
31	GPIO3	I/O	Digital I/O Pin
32	GPIO1	I/O	Digital I/O Pin
33	GND	G	Exposed Ground pad, needs to be grounded

4 Interface description

MCU or other controllers can configure the registers and FIFOs of PAN3028 via SPI.

4.1 SPI

Only SPI slave side is implemented in PAN3028.

The SPI buses are four-wire, as follows:

- SCK (Clock)
- CSN (Chip Select, Low level active)
- MOSI (Input）
- MISO (Output)

SCK, CSN, and MOSI are controlled by the Master. MISO is controlled by Slave.

The communication process starts with the pulling down of CSN level and ends with the pulling up of CSN level. The Master sends data by MOSI, and receives data from MISO. Data is generated on the falling edge of SCK, and is sampled on the rising edge.

The information transmitted by the Master consists of Address Byte and Data Byte. The first 7 bits of the Address Byte are the address bits. The last 1 bit is the read/write bit, which is set to 1 during the write operation and 0 during the read operation.

SPI has three transfer modes：

- Single: Single-byte Transfer Mode. The length of information is only 2 bytes. The Master sends the Address Byte by MOSI. In writing operation, the Master continues to send the Data Byte by MOSI. If in reading operation, the Master reads the Data Byte replied by the Slave on the MISO.
- Burst: Burst Continuous Transfer Mode. If the information is longer than 2 bytes, the Address Byte is followed by several Data Bytes. There is no need to add an Address Byte between the Data Bytes. The Slave will automatically increment the address between each Data Byte. The CSN signal is pulled high after the last Data Byte. During the rest of the information transmission process CSN remains low.
- FIFO: FIFO Read and Write Mode. In this mode, single-byte or continuous transmission can be realized. The transmission rules are the same as those in Signle mode and Burst mode. The difference is that the address bit *addr* in Address Byte shall only be configured as 7'h1, and Slave does not increment address between Data Bytes.

  SPI write timing diagram is as follows.

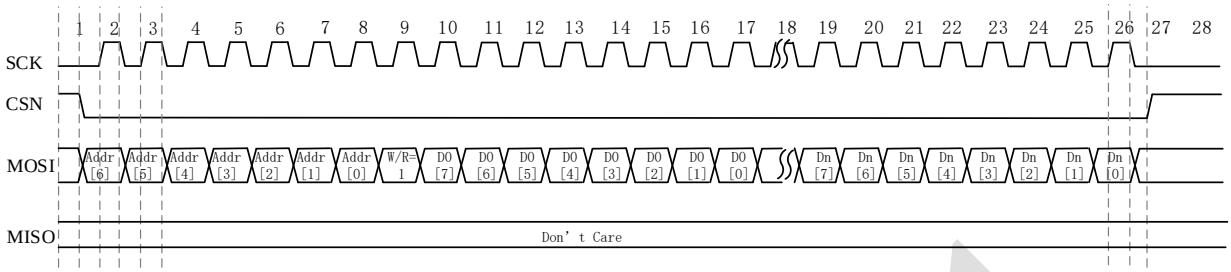

Figure 4-1 SPI write timing

SPI read timing diagram is as follows.

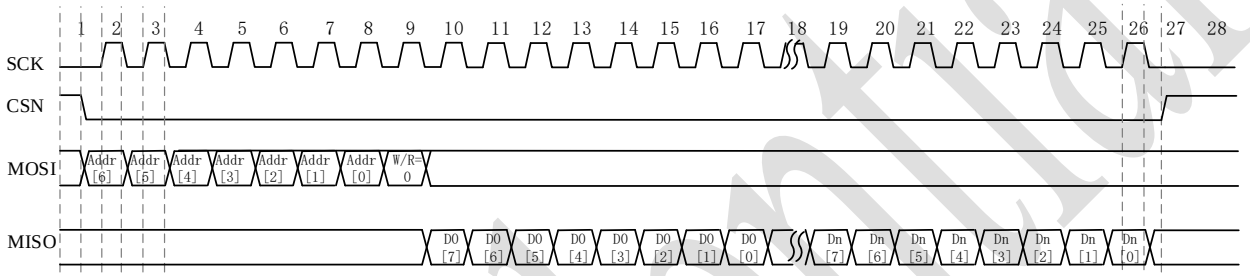

Figure 4-2 SPI read timing

4.2 FIFO

PAN3028 has a FIFO of 256 bytes to store the data sent by the TX module and the decoded data sent by the RX module.

The FIFO is composed of a single-port RAM, which can only store and read a single packet of data information. If there is a packet of data stored in the FIFO, the data of this packet should be read before writing. Otherwise, the previous packet of data in the FIFO will be overwritten.

In the mode of STB3 and the later, the FIFO can be read and written by Modem and SPI.

5 Electrical Characteristics

All parameters are accurate to one decimal place.

5.1 Absolute Maximum Ratings

Test Conditions:

- Supply voltage: 3.3V
- Temperature: 25℃

Table 5-1 Absolute Maximum Ratings

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
VDD	VDD1/VDD2/VDD3/VBAT/VBAT_IO	-0.3	3.3	3.6	V
V_I	Input voltage	-0.3	-	VDD	V
V_O	Output voltage	VSS	-	VDD	V
T_{OP}	Operating temperature	-40	-	85	℃
T_{STG}	Storage temperature	-55	-	125	℃

Note:

- Exceeding one or more maximum ratings may cause permanent damage to PAN3028.
- Electrostatic sensitive equipment, operate in accordance with the protection rules.

5.2 Current Consumption

Test Conditions:

- Supply voltage: 3.3V
- Temperature: 25℃
- Frequency: 490MHz

Table 5-2 Voltage and Current

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
VDD	Power supply voltage	1.8	3.3	3.6	V	TA=25℃, non-DCDC mode
		2	3.3	3.6	V	TA=25℃, DCDC mode
VSS	Ground	-	0	-	V	-
$I_{DeepSleep}$	Deep sleep mode current	-	400	-	nA	-
$I_{TX,22dBm}$	Operating current in TX mode	-	135	-	mA	22dBm output power
$I_{TX,18dBm}$		-	83	-	mA	18dBm output power
$I_{TX,0dBm}$		-	25	-	mA	0dBm output power
$I_{RX,DCDC}$	Operating current in RX mode	-	12.5	-	mA	Max LNA gain in DCDC mode
$I_{RX,LDO}$	Operating current in RX mode	-	18	-	mA	Max LNA gain in LDO Mode
V_{OH}	Output high level voltage	VDD-0.3	-	VDD	V	-
V_{OL}	Output low level voltage	VSS	-	VSS+0.3	V	-

V_{IH}	Input high level voltage	0.8*VDD	-	-	V	-
V_{IL}	Input low level voltage	-	-	0.2*VDD	V	-
SPI_rate	SPI rate	-	-	10	Mbps	-

5.3 RF performance

Test Conditions:

- Supply voltage: 3.3V
- Temperature: 25℃
- Frequency: 490MHz
- Error Correction Code = 4/8
- Packet error rate ≤ 5%
- Payload length = 10Bytes

Table 5-3 RF parameters

Symbol	Description	Condition	Min	Typ	Max	Unit
General frequency						
F_{op}	Operating frequency	-	370	-	590	MHz
		-	740	-	1180	MHz
F_{xtal}	Crystal frequency	-	-	32	-	MHz
R_S	Crystal series resistance	-	-	30	50	Ω
C_{FOOT}	Crystal external capacitor	-	8	15	22	pF
C_{LOAD}	Crystal load capacitance	-	6	10	12	pF
F_{TOL}	Initial frequency tolerance	-	-	±10	-	ppm
BR	Bit rate		0.08	-	20.4	kbps
Transmitter						
P_{LPWAN}	Output Power	-	-23.5	-	22	dBm
Receiver						
RF_62.5	RF sensitivity, long range mode, highest LNA gain, 62.5 kHz bandwidth using separate RX/TX channels	SF = 7 SF = 10 SF = 12	- - -	-126 -135 -140	- - -	dBm
RF_125	RF sensitivity, long range mode, highest LNA gain, 125 kHz bandwidth using separate RX/TX channels	SF = 7 SF = 10 SF = 12	- - -	-124 -132 -137	- - -	dBm
RF_250	RF sensitivity, long range mode, highest LNA gain, 250 kHz bandwidth using separate RX/TX channels	SF = 7 SF = 10 SF = 12	- - -	-121 -129 -134	- - -	dBm
RF_500	RF sensitivity, long range mode, highest LNA gain, 500 kHz bandwidth using separate RX/TX channels	SF = 7 SF = 10 SF = 12	- - -	-119 -126 -132	- - -	dBm

Note:

- The above test data is based on the 490MHz frequency point. There are differences in other frequency band parameters.

6 Application Reference Diagram

6.1 Application Reference Diagram

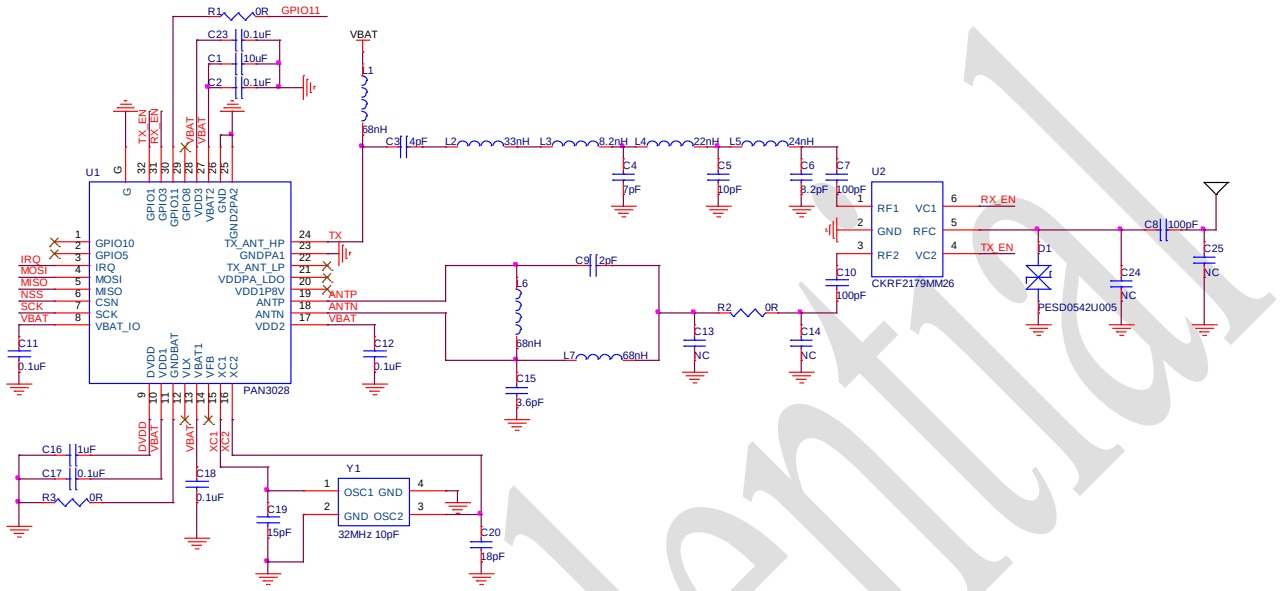

Figure 6-1 Application Schematic of the PAN3028（External LDO power supply）

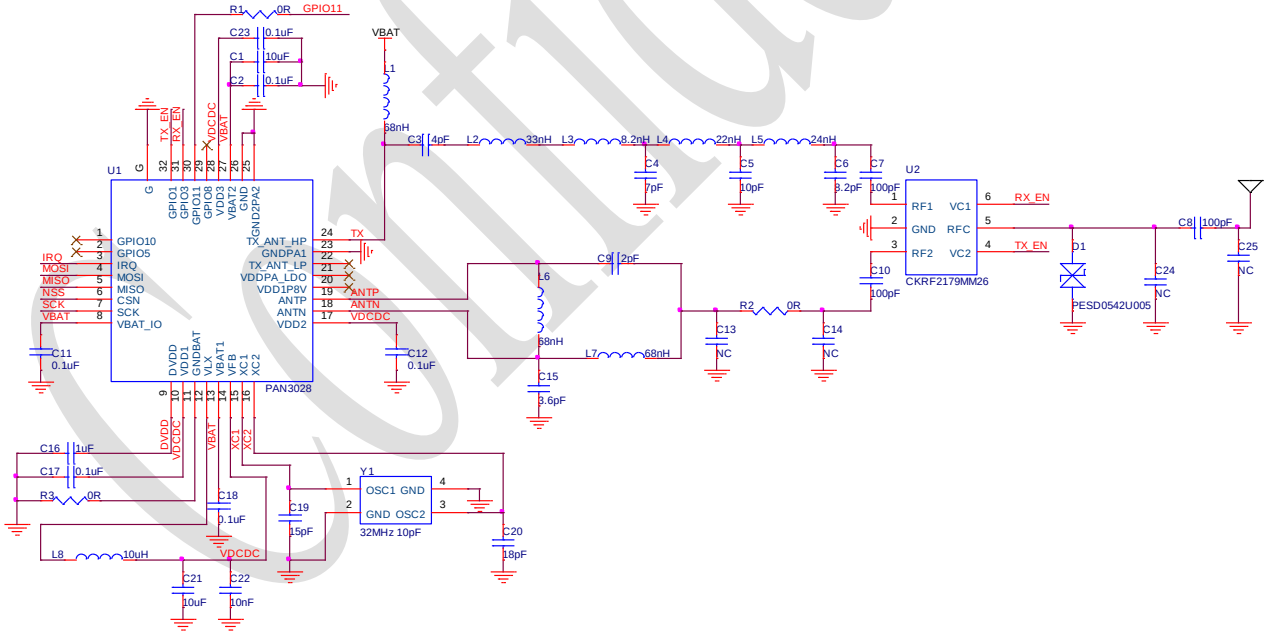

Figure 6-2 Application Schematic of the PAN3028（Internal DCDC power supply）

Note:

- VBAT_IO supplies power to the chip GPIO and determines the reference level of the GPIO. When using DCDC power supply, GNDBAT needs to use a 0R resistor to ground at a single point.

6.2 Reference values for different frequency band matching

Frequency（MHz）	TX								
	L1(nH)	C3(pF)	L2(nH)	L3(nH)	C4(pF)	L4(nH)	C5(pF)	L5(nH)	C6(pF)
433	68	4	33	8.2	7	22	10	24	8.2
470~510	68	3	33	10	12	27	9	24	2.7
863~870	220	2.2	15	5.1	5	12	6	9.1	3.9
902~928	220	2.2	15	5.1	5	15	6	8.2	3.9

Note:

1. L3, C4, L4, C5, L5, and C6 are filter matching for safety regulations, and can be removed if safety regulations are not considered.
2. Matching component values need to be fine-tuned according to TR Switch and Layout.
3. The inductor L1 is recommended to use a device with a DC internal resistance less than 2 ohms and a rated current greater than 150mA.

Frequency（MHz）	RX			
	L6(nH)	C9(pF)	L7(nH)	C15(pF)
433	68	2	68	3.6
470~510	56	1.5	56	3
863~870	15	3	56	1.8
902~928	15	3	56	1.8

Note:

1. Matching component values need to be fine-tuned according to TR Switch and Layout.
2. For configuration values of other frequency bands, please refer to the hardware design reference document.

7 Package Dimensions

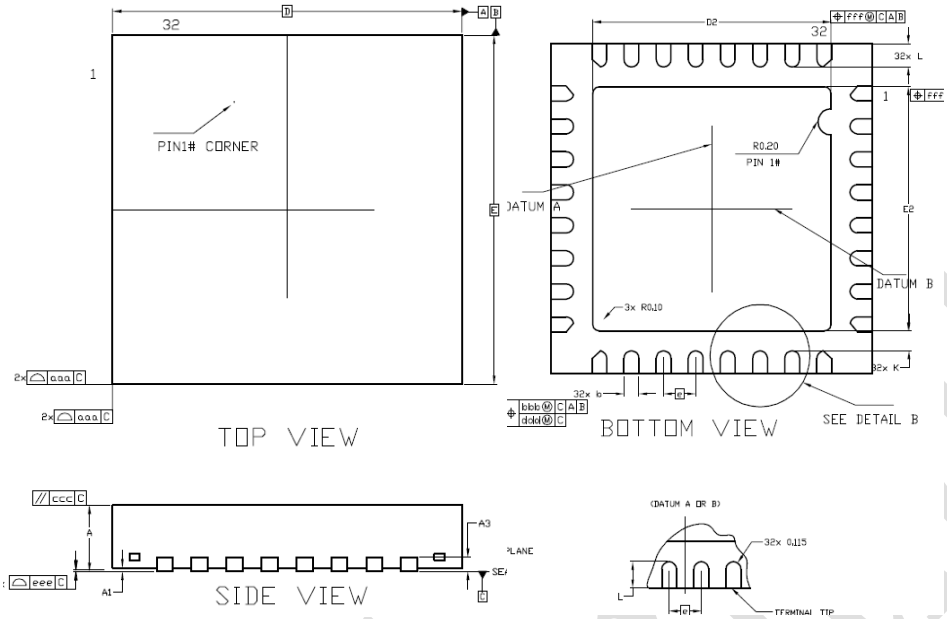

Figure 7-1 QFN32 5*5 Package View

Table 7-1 QFN32 5*5 Package Dimension

SYMBOL	MIN(mm)	NOM(mm)	MAX(mm)
A	0.70	0.75	0.80
	0.85	0.90	0.95
A1	0	0.02	0.05
A3	-	0.20 REF	-
b	0.18	0.23	0.28
D	5.00BSC		
E	5.00BSC		
D2	3.55	3.65	3.75
E2	3.55	3.65	3.75
e	0.50BSC		
L	0.30	0.35	0.40
K	0.20	-	-
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

8 Precautions

1) This product is a CMOS device and should be protected against static electricity during storage, transportation and use.
2) Grounding when device is in use.
3) Reflow temperature can not exceed 260℃.

   The lead-free reflow soldering process is shown in the figure below:

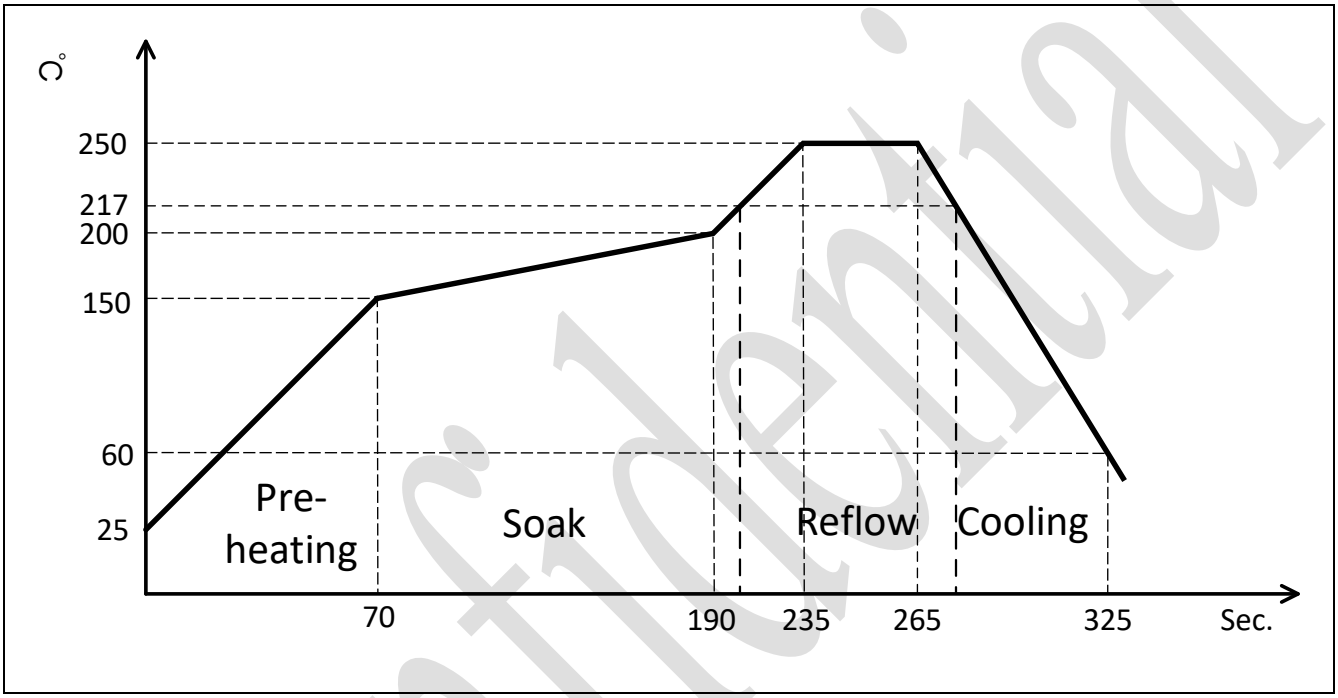

Figure 8-1 Reflow Profile

9 Storage Conditions

1) Products should be stored in sealed packages: when the temperature is less than 30 degrees and the humidity is less than 90%, it can last for 12 months.

2) After the package is opened, the components will be used in the reflow process or other high-temperature processes. The following conditions must be met:

   a) Completed within 72 hours and the factory environment is less than 30℃≤ 60% RH.

   b) Stored in 10% RH environment.

   c) Exhaust at 125℃ for 24 hours to remove internal water vapor before used.

3) MSL (Moisture Sensitivity Level): Level-3 (based on IPC/JEDEC J-STD-020)