PAN159CY Serials Product Manual

32-bit 2.4G RF Transceiver SOC

General Description

PAN159CY is an 32-bit 2.4GHz Transceiver SOC. It is designed for operation in the world wide ISM frequency band at 2.400~2.483GHz,integrating radio frequency (RF) transmitter and receiver, frequency synthesizer, crystal oscillator, baseband GFSK modem, and so on,supporting one to multiple network and communication with ACK. TX power, frequency channel, and data rate can be set. Multiple external components are integrated into the chip. 32 KB Flash memory for program memory 2 KB Flash for loader and 4 KB SRAM are inside, one up to 12 channels. PAN159 also provides 23 IO、8 channels ADC 、6 channels PWM.

Main Features

1、CPU

ARM Cortex-M0 core running up to 50 MHz；

32 KB Flash for APROM，4 KB SRAM，2KB Flash for LDROM；

2、RF Module

Supporting automatic reply and automatic retransmission；

1Mbps 250kbps optional data rate in air；

Programmable Output Power from -5dBm to 13dBm；

Excellent Receiver sensitivity -87dBm@1Mbps ,-91dBm@250Kbps；

3、Others

Clock：Built-in 22.1184 MHz HIRC,10 kHz LIRC；

Provides two channel 32-bit Timers；

Up to three built-in 16-bit PWM generators，providing 6 PWM outputs or three complementary paired PWM outputs；

LVR： 2.0V；

Two analog Comparators with programmable 16-level internal voltage reference；

BOD：With 4 programmable threshold levels： 4.4V/3.7V/2.7V/2.2V；

ADC：10-bit SAR ADC;

Operating voltage range：2.2V ~3.3V；

Operating temperature range：-40℃ ~ 85℃；

Package information:

PAN159CY: QFN40 (5*5);

RoHS(Green)

Application

Four axis rotor saucer

Revision	Data	Description	Related documents
V1.0	2016.05	Draft	《01_XN297L serials Datasheet _V4p7》 《TRM_Mini58DE_Series_EN_Rev1.00》

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1 Block Diagram

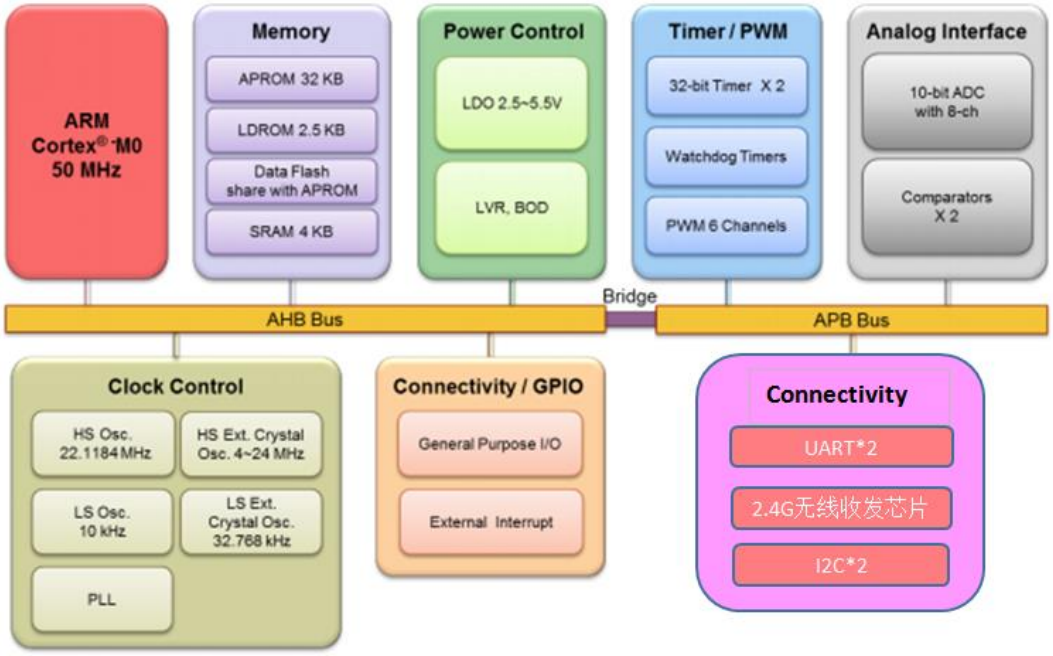


Figure 1 PAN159 block diagram

2 Pin Definition and Functional Description

2.1 Pin Definition

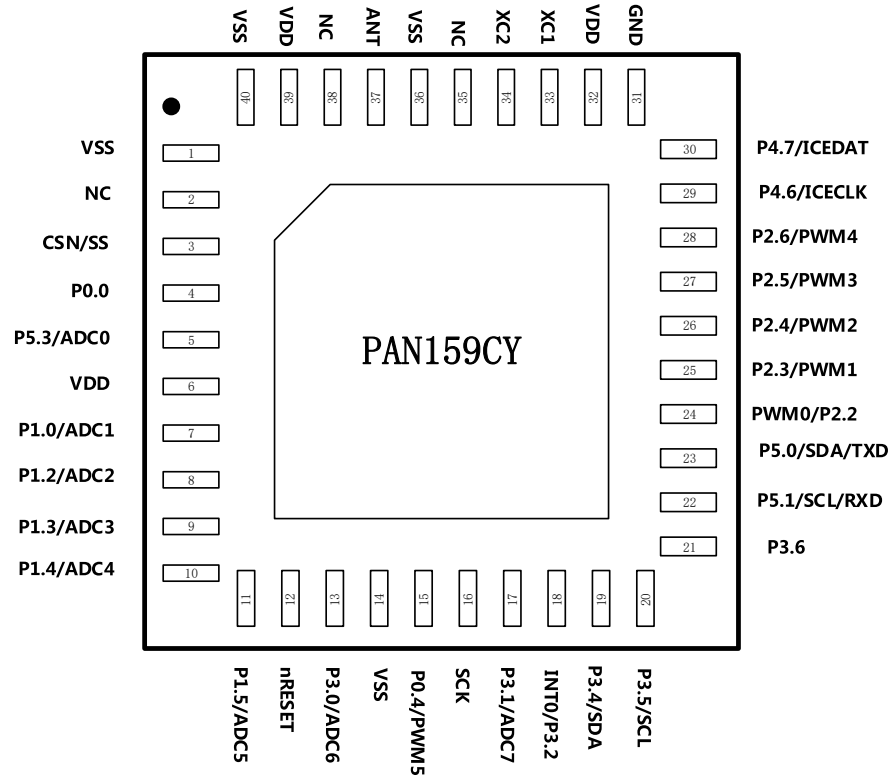


Figure 2.1 PAN159 pins

2.2 Functional Description

rogram writing pins：p4.6/p4.7/nRESET

Table 2.2 functional description

NO	Pin name	Pin&Buffer Typ	Description
1	VSS	G	GND
2	NC	---	
3	CSN/SS	---	SPI CHIP SELECT
4	P0.0	I/O	General purpose digital I/O
5	P5.3	I/O	General purpose digital I/O
	ADC_CH0	AI	ADC analog input
6	VDD	P	Power
7	P1.0	I/O	General purpose digital I/O
	ADC_CH1	AI	ADC analog input
8	P1.2	I/O	General purpose digital I/O
	ADC_CH2	AI	ADC analog input
	UART0_RXD	I	UART0 data input
	PWM0_CH0	O	PWM0 output

9	P1.3	I/O	General purpose digital I/O
	ADC_CH3	AI	ADC analog input
	UART0_TXD	O	UART0 data output
	PWM0_CH1	O	PWM1 output
10	P1.4	I/O	General purpose digital I/O
	ADC_CH4	I/O	ADC analog input
	UART1_RXD	I	UART1 data input
	PWM0_CH4	O	PWM4 output
11	P1.5	I/O	General purpose digital I/O
	ADC_CH5	I/O	ADC analog input
	UART1_TXD	O	UART1 data output
12	nRESET	---	nRESET
13	P3.0	I/O	General purpose digital I/O
	ADC_CH6	AI	ADC analog input
14	VSS	G	GND
15	P0.4	I/O	General purpose digital I/O
	PWM0_CH5	O	PWM5 output
16	SCK/SCK_RF	---	SPI clock
17	P3.1	I/O	General purpose digital I/O
	ADC_CH7	I/O	ADC analog input
18	P3.2	I/O	General purpose digital I/O
	INT0	I	External interrupt 0 input
19	P3.4	I/O	General purpose digital I/O
	I2C0_SDA	I/O	I2C0 data input/output
20	P3.5	I/O	General purpose digital I/O
	I2C0_SCL	I/O	I2C0 clock
21	P3.6	I/O	General purpose digital I/O
22	P5.1	I/O	General purpose digital I/O
	I2C1_SCL	I/O	I2C1 clock
	UART0_RXD	I	UART0 data intput
23	P5.0	I/O	General purpose digital I/O
	I2C1_SDA	I/O	I2C1 data input/output
	UART0_TXD	O	UART0 data output
24	P2.2	I/O	General purpose digital I/O
	PWM0_CH0	O	PWM0 output
	I2C1_SCL	I/O	I2C1 clock
25	P2.3	I/O	General purpose digital I/O
	PWM0_CH1	O	PWM1 output
	I2C1_SDA	I/O	I2C1 data input/output
26	P2.4	I/O	General purpose digital I/O

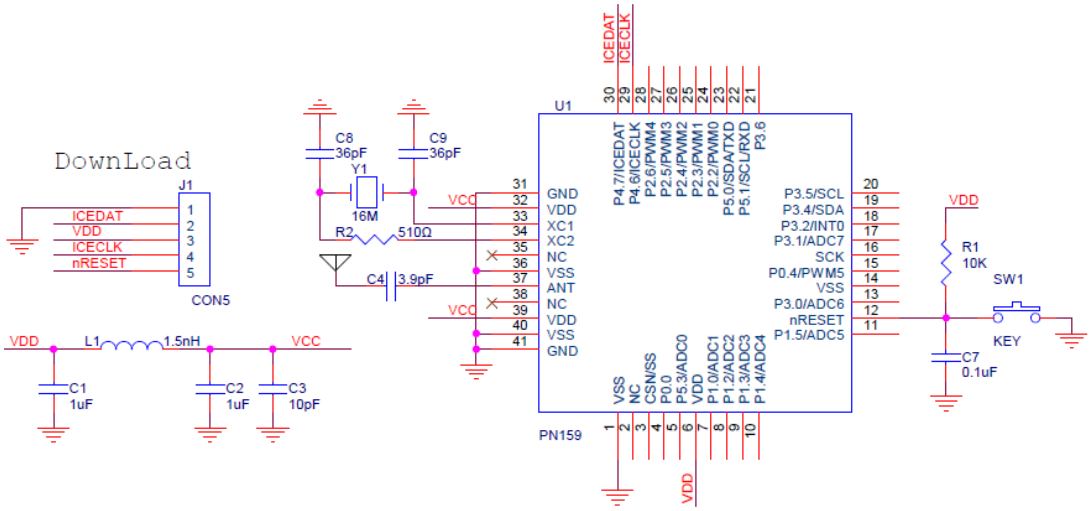
	UART1_RXD	I	UART1 data input
	PWM0_CH2	O	PWM2 output
27	P2.5	I/O	General purpose digital I/O
	UART1_TXD	O	UART1 data output
	PWM0_CH3	O	PWM3 output
28	P2.6	I/O	General purpose digital I/O
	PWM0_CH4	O	PWM4 output
29	P4.6	I/O	General purpose digital I/O
	ICE_CLK	I	Programming Clock
	UART1_RXD	I	UART1 data input
30	P4.7	**I/O**	General purpose digital I/O
	ICE_DAT	**I/O**	Programming Data
	UART1_RXD	**O**	UART1 data output
31	GND	G	GND
32	VDD	P	Power
33	XC1	AI	Crystal Pin 1
34	XC2	AO	Crystal Pin 2
35	NC	---	NC
36	VSS	G	GND
37	ANT	AIO	Antenna interface
38	NC	---	NC
39	VDD	P	Power
40	VSS	G	GND

2.3 Inter Connection

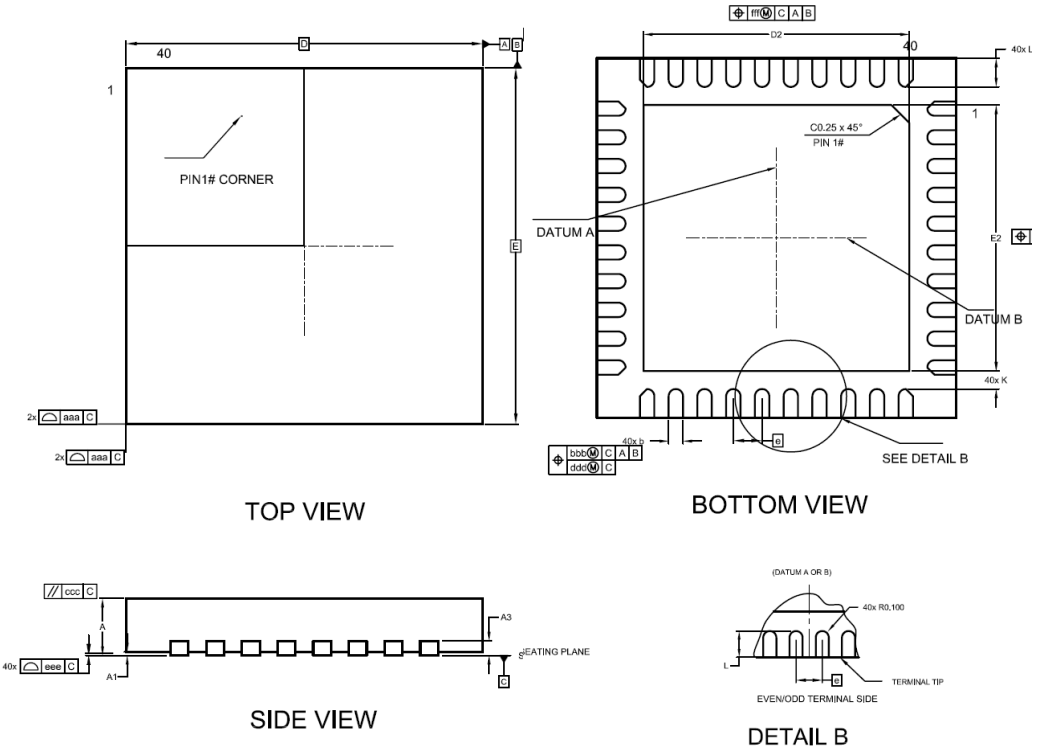
Table 2.3 inter connection

Pin Status	RF	MCU
I S	MISO	P0.6
I S	MOSI	P0.5
I S	IRQ	P5.2
Pin16	SCK	P0.7
Pin3	CSN	P0.1

3 Apllication examples



4 Package Size



DIM / SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
	0.85	0.90	0.95
A1	0	0.02	0.05
A3	-	0.20 REF	-
b	0.15	0.20	0.25
D	5.0BSC		
E	5.0BSC		
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.40BSC		
L	0.35	0.40	0.45
K	0.20	-	-
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure3.1 PAN159 package size