Panchip Microelectronics Co., Ltd.

XN297L

Datasheet

Single Chip 2.4GHz Transceiver

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REVISION HISTORY

Version	Date	Description
V4.8	May 2016	Added details of the following features: ● SPI rate-adjustment ● Power down mode ● Standby-I mode
V4.9	Apr 2022	Add Precautions & Storage Conditions.
V5.0	Jun 2022	Add XN297LCV
V5.1	Aug 2022	Update the value of VIH/VIL in DC Characteristics
V5.2	Sep 2022	Add Ordering Information
V5.3	Jun 2023	Add XN297LCW. Add the reflow profile and the MSL level
V5.4	Oct 2023	Updating clerical error. Revise the last paragraph of the description in the General Description.
V5.5	Apr 2024	Update the Package Dimensions of the SOP16 package.
V5.6	Nov 2024	Add SPI read/write mode.

Ordering Information

Part number	Marking	Package	Pin count	Packing
XN297LCD	/	DICE	/	Case
XN297LCQH	XN297LCU	QFN	20	Tape & Reel
XN297LBSB	XN297LBW	SOP	8	Tape & Reel
	XN297LCW	SOP	8	Tape & Reel
XN297LCSF	XN297LCV	SOP	16	Tube

MSL (Moisture Sensitivity Level): Level-3 (based on IPC/JEDEC J-STD-020)

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Abbreviation

ACK	Acknowledgment
BER	Bit Error Rate
CRC	Cyclic Redundancy Check
FIFO	First Input First Output
GFSK	Gauss frequency Shift Keying
ISM	Industrial Scientific Medical
LSB	Least significant bit
MCU	Microcontroller Unit
PID	Packet identification
PLL	Phase Locked Loop
PRX	Primary Receiver
PTX	Primary Transmitter
RF	Radio Frequency
RFID	Radio Frequency Identification
RSSI	Received Signal Strength Indication
SPI	Serial Peripheral Interface
STB	Set Top Box
TDD	Time Division Duplexing

1 General Description

XN297L is a single chip 2.4GHz RF transceiver designed for operation in the world wide ISM frequency band from 2.400 to 2.483GHz. XN297L with an embedded baseband protocol engine, is suitable for ultra-low power wireless applications.

XN297L is a highly integrated RF transceiver which composes of only an MCU (microcontroller) and a few external passive components and can be used to build up a radio system for wireless applications. XN297L is operated and configured through a Serial Peripheral Interface (SPI). All of registers are accessible through SPI in the read/write operation modes.

XN297L operates in TDD mode, either as a transmitter or as a receiver. The embedded baseband engine supports various modes from normal BURST to enhanced BURST, based on the packet communication. Internal FIFOs ensures a smooth data flow between the radio front and the system's MCU. Enhanced BURST reduces system cost by handling all the high speed link layer operations. XN297L employs GFSK modulation and the RF parameters such as frequency channel, output power and interface data rate can be configured. XN297L supports an data rate of 2Mbps, 1Mbps and 250Kbps. The output power can be adjusted up to 11dBm for a long distance application, or below to -23dBm for a short range and ultra-low power application.

The current version is compatible with earlier versions of the XN297, which has fewer external passive components than the XN297.

1.1 Key Features

- Radio
  - Frequency band: 2.400 ~ 2.483GHz
  - Data rate: 2Mbps, 1Mbps and 250kbps
  - GFSK modulation
- RF Synthesizer
  - Fully integrated synthesizer
  - Accept low cost ±60ppm 16MHz crystal for the data rate of 1Mbps and 2Mbps
  - Accept low cost ±20ppm 16MHz crystal for the data rate of 250Kbps
- Transmitter
  - Programmable output power: 11, 9, 5, -1, -10 or -23dBm
  - 18mA at 2dBm output power
  - 30mA at 9dBm output power
- Receiver
  - -83dBm sensitivity at 2Mbps
  - -87dBm sensitivity at 1Mbps
  - -91dBm sensitivity at 250Kbps
- Protocol engine
  - Support 1 to 32 or 64 byte payload length
  - Support automatic reply and automatic retransmission

- 6 data pipes receive for 1:6 star networks

- Power Management
  - Integrated voltage regulator
  - 2.3 to 3.3V supply range
  - 2uA power down mode
  - 30uA Standby-I mode
- Host Interface
  - Support 4-pin and 3-pin SPI
  - Up to 4Mbps SPI interface rate
  - Support two separate 32 bytes TX and RX FIFOs
  - Support one 64 bytes TX and RX FIFOs
- Package
  - SOP8 package
  - SOP16 package
  - Compact 20-pin 3×3mm QFN package

1.2 Block Diagram

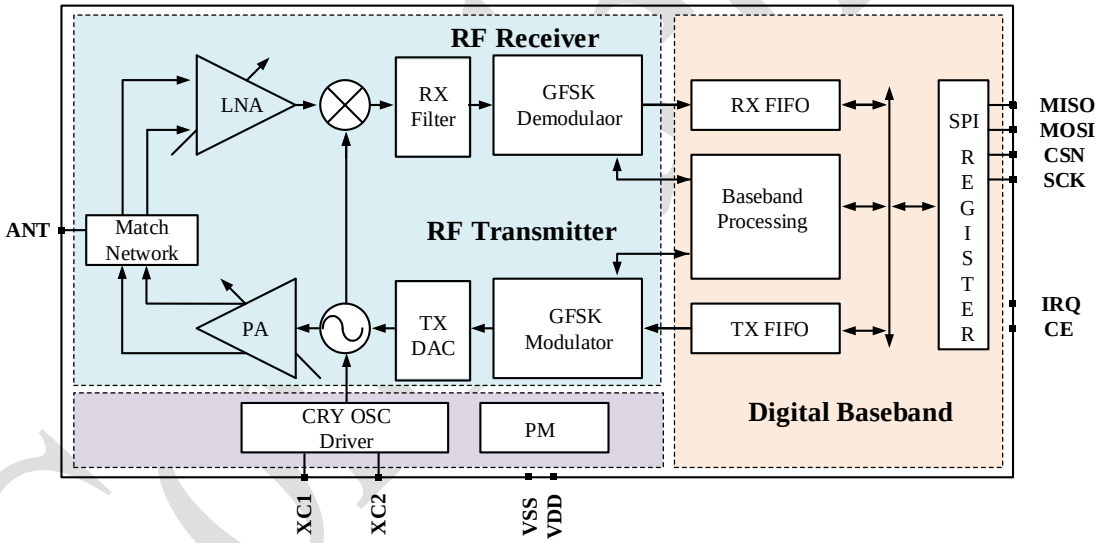

Figure 1-1 XN297L block diagram

1.3 Typical Applications

- TV and STB remote controls
- Wireless mouse and keyboard
- Toys and wireless audio
- Wireless gamepads
- Active RFID
- Smart home automation

2 Pin Information

2.1 Pin Assignment and Pin Descriptions

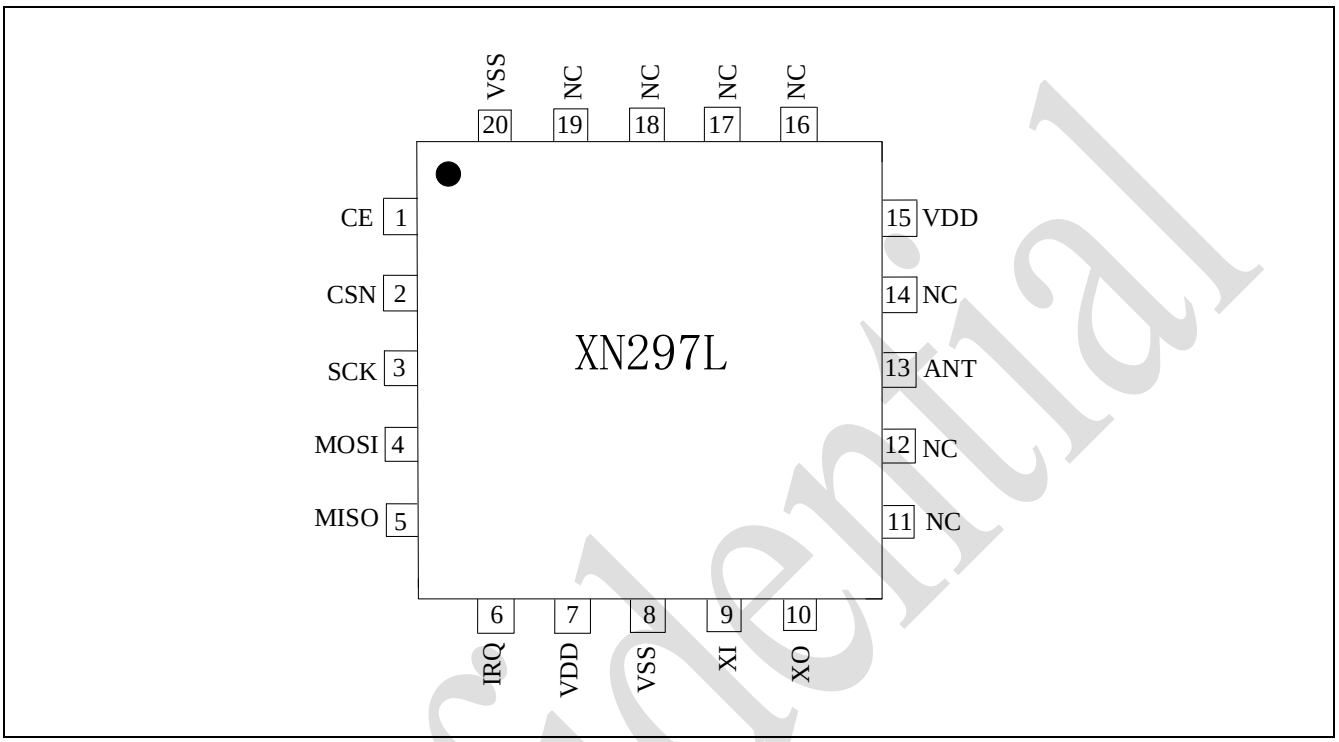

Figure 2-1 Pin assignment for the QFN20 3×3 package

Table 2-1 Pin function for the QFN20 pin 3×3 package

PIN	Name	Description	PIN	Name	Description
1	CE	Mode Chip Select Signal	11	NC	/
2	CSN	SPI Chip Select	12	NC	/
3	SCK	SPI Clock	13	ANT	Antenna Interface
4	MOSI	SPI Data Input	14	NC	/
5	MISO	SPI Data Output	15	VDD	Power Supply(+2.3~+3.3V DC)
6	IRQ	Maskable interrupt pin.	16	NC	/
7	VDD	Power Supply(+2.3~+3.3V DC)	17	NC	/
8	VSS	Ground(GND)	18	NC	/
9	XC1	Crystal Oscillator Input	19	NC	/
10	XC2	Crystal Oscillator Output	20	VSS	Ground(GND)

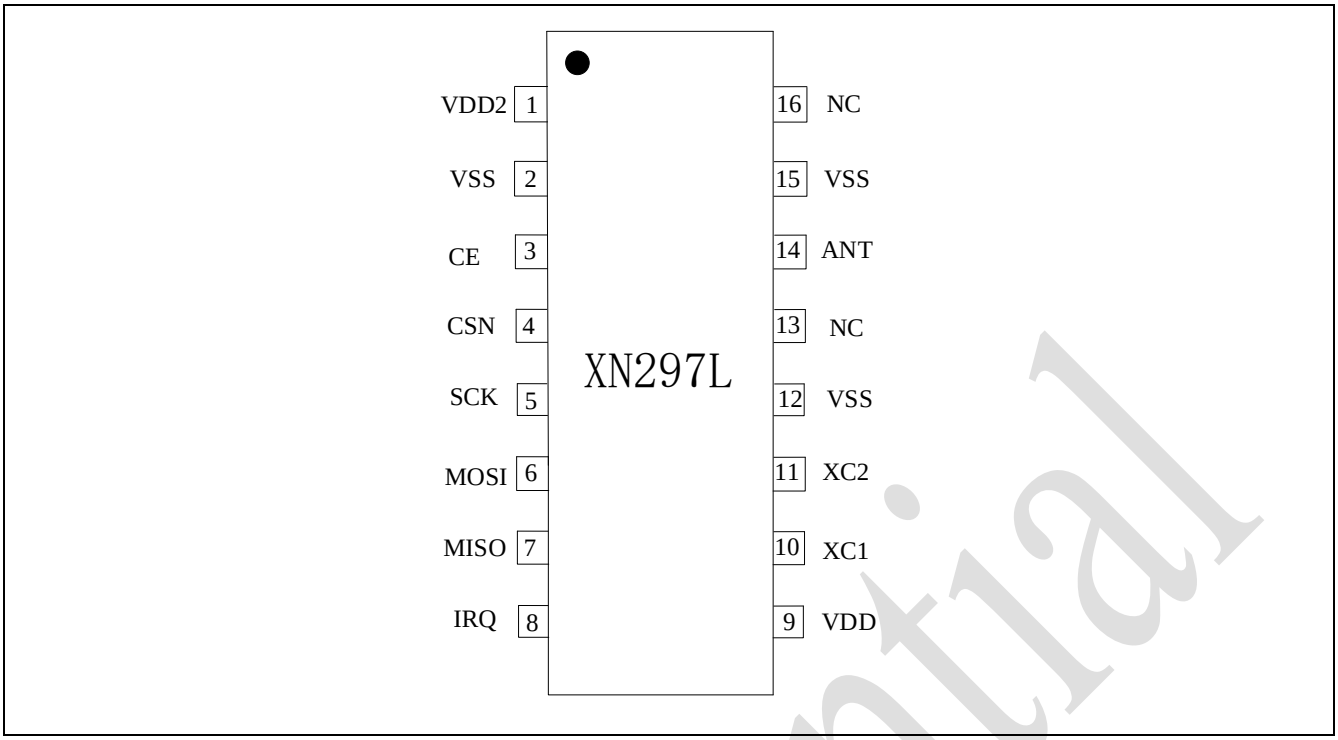

Figure 2-2 Pin assignment for the SOP16 package

Table 2-2 Pin function for the SOP16 package

PIN	Name	Description	PIN	Name	Description
1	VDD2	Power Supply	9	VDD	Power Supply
2	VSS	Ground(GND) NC could be optional	10	XC1	Crystal Oscillator Input
3	CE	Mode Chip Select Signal	11	XC2	Crystal Oscillator Output
4	CSN	SPI Chip Select	12	VSS	Ground(GND) NC could be optional
5	SCK	SPI Clock	13	NC	/
6	MOSI	SPI Data Input	14	ANT	Antenna Interface
7	MISO	SPI Data Output	15	VSS	Ground(GND)
8	IRQ	Maskable interrupt pin.	16	NC	/

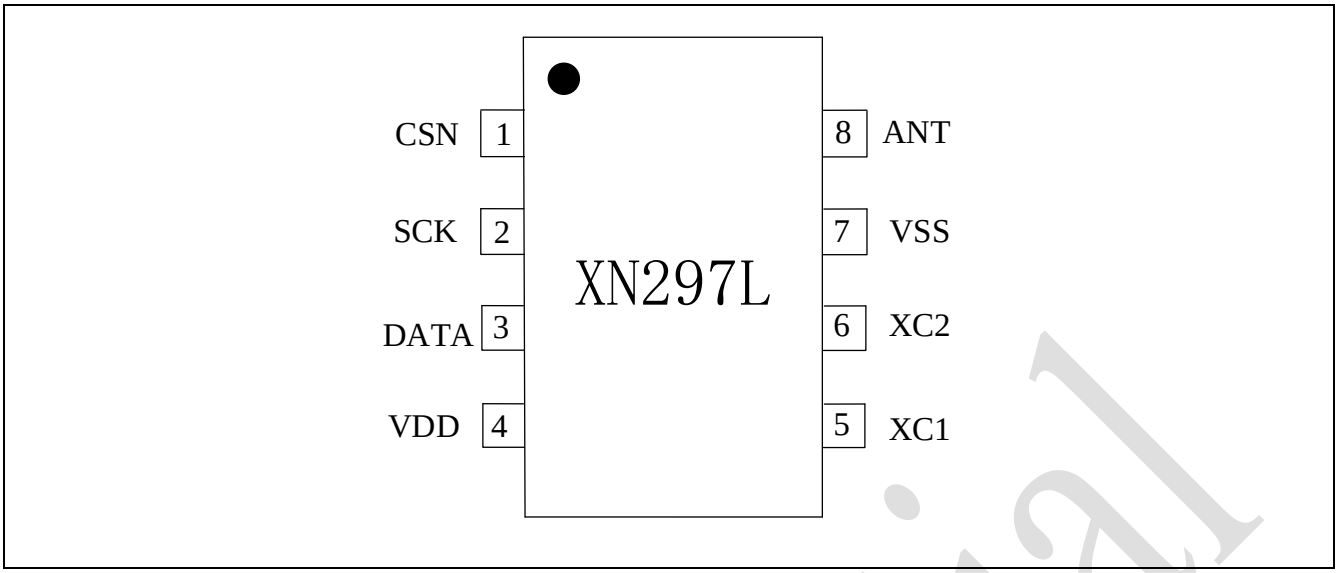

Figure 2-3 Pin assignment for the SOP8 package

Table 2-3 Pin function for the SOP8 package

PIN	Name	Description	PIN	Name	Description
1	CSN	SPI Chip Select	5	XC1	Crystal Oscillator Input
2	SCK	SPI Clock	6	XC2	Crystal Oscillator Output
3	DATA	SPI Slave Data Input/Output	7	VSS	Ground(GND)
4	VDD	Power Supply(+2.3~+3.3V DC)	8	ANT	Antenna interface

3 Electrical Specification

Conditions: VDD=+3V, VSS=0V, TA=25℃

3.1 Absolute Maximum Ratings

Table 3-1 Absolute maximum ratings

Symbol	Parameter(Condition)	Min	Max	Units
V_{DD}	Supply voltage	-0.3	3.6	V
V_I	Input voltage	-0.3	3.6	V
V_O	Output voltage	VSS	VDD	-
Pd	Total Power Dissipation （TA=-40℃~85℃）	-	300	mW
T_{OP}	Operating Temperature	-40	85	℃
T_{STG}	Storage Temperature	-40	125	℃

Note: Exceeding one or more of the limiting values may cause permanent damage to XN297L.

3.2 Current Consumption

Table 3-2 Current consumption

Symbol	Parameter (Condition)	Min	Type	Max	Unit
ICC	Power-down	-	2	-	uA
	Standby I	-	30	-	uA
	Standby III	-	650	-	uA
	Standby II	-	780	-	uA
	TX at -35dBm Output Power	-	9	-	mA
	TX at -20dBm Output Power	-	9.5	-	mA
	TX at 0dBm Output Power	-	16	-	mA
	TX at 2dBm Output Power	-	19	-	mA
	TX at 8dBm Output Power	-	30	-	mA
	TX at 13dBm Output Power	-	66	-	mA
	RX at 2Mbps	-	16.5	-	mA

	RX at 1Mbps	-	15.5	-	mA
	RX at 250kbps	-	15	-	mA

3.3 General RF Conditions

Table 3-3 General RF conditions

Symbol	Parameter(Condition)	Min	Type	Max	Unit
f_{OP}	Operating Frequency	2400	-	2483	MHz
PLL_{res}	PLL Programming Resolution	-	1	-	MHz
f_{XTAL}	Crystal Frequency	-	16	-	MHz
DR	Data Rate	0.25	-	2	Mbps
Δf_{250K}	Frequency Deviation at 250kbps	-	150	180	KHz
Δf_{1M}	Frequency Deviation at 1Mbps	-	160	300	KHz
Δf_{2M}	Frequency Deviation at 2Mbps	-	320	550	KHz
FCH_{250K}	Channel Spacing at 250Kbps	-	1	-	MHz
FCH_{1M}	Channel Spacing at 1Mbps	-	1	-	MHz
FCH_{2M}	Channel Spacing at 2Mbps	-	2	-	MHz

Note1: The channels, which is integer times of 16MHz, such as 2400 MHz, 2416 MHz, 2432 MHz, 2448 MHz, 2464 MHz, and 2480MHz is not recommended. Because of the receiver sensitivity is degraded about 2dB in these channels.

3.4 Transmitter Operation

Table 3-4 Transmitter operation

Symbol	Parameter(Condition)	Min	Type	Max	Unit
PRF	Typical Output Power	2	8	11	dBm
$PRFC$	Output Power Range	-35	-	11	dBm
$PBW1$	20db Bandwidth For Modulated Carrier at 2Mbps	-	2	-	MHz
$PBW2$	20db Bandwidth For Modulated	-	1	-	MHz

	Carrier at 1Mbps				
$PBW3$	20db Bandwidth For Modulated Carrier at 250Kbps	-	500	-	KHz

3.5 Receiver Operation

Table 3-5 Receiver operation

Symbol	Parameter(Condition)	Min	Type	Max	Unit
RX_{max}	Maximum Received Amplitude at <0.1% BER	-	0	-	dBm
$RXSENS1$	Sensitivity (0.1%Ber) @2mbps	-	-83	-	dBm
$RXSENS2$	Sensitivity (0.1%Ber) @1mbps	-	-87	-	dBm
$RXSENS3$	Sensitivity (0.1%Ber) @250kbps	-	-91	-	dBm
C/I_{CO}	C/I Co-Channel (@2Mbps)	-	10	-	dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I	-	-6	-	dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I	-	-10	-	dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I	-	-22	-	dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I	-	-28	-	dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I	-	-34	-	dBc
C/I_{CO}	C/I Co-Channel (@1Mbps)	-	10	-	dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I	-	1	-	dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I	-	-18	-	dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I	-	-23	-	dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I	-	-28	-	dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I	-	-32	-	dBc
C/I_{6TH}	6th Adjacent Channel Selectivity C/I	-	-35	-	dBc

C/I_{CO}	C/I Co-Channel (@250Kbps)	-	2	-	dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I	-	-8	-	dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I	-	-18	-	dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I	-	-24	-	dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I	-	-28	-	dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I	-	-32	-	dBc
C/I_{6TH}	6th Adjacent Channel Selectivity C/I	-	-35	-	dBc

3.6 DC Characteristics

Table 3-6 DC characteristics

Symbol	Parameter(Condition)	Min	Type	Max	Unit
VDD	Supply Voltage	2.3	3	3.3	V
VSS	Ground	-	0	-	V
V_{OH}	Output High Level Voltage	VDD-0.3	-	VDD	V
V_{OL}	Output Low Level Voltage	VSS	-	VSS+0.3	V
V_{IH}	Input High Level Voltage	0.7*VDD	-	VDD	V
V_{IL}	Input Low Level Voltage	VSS	-	0.3*VDD	V

4 Operational Modes

This chapter describes all kinds of operating modes of XN297L and the methods used to control the chip into each mode of operation. The XN297L chip's own state machine is controlled by the configuration values of the chip's internal registers and external pin signals.

4.1 State Diagram

The state diagram in Figure 4-1 shows 5 kinds of operating modes and how they jump. The XN297L starts to work normally when VDD is greater than 2.2V. Even if it enters power down mode, the MCU can send configuration commands through the SPI and CE pins to put the chip into the other five states.

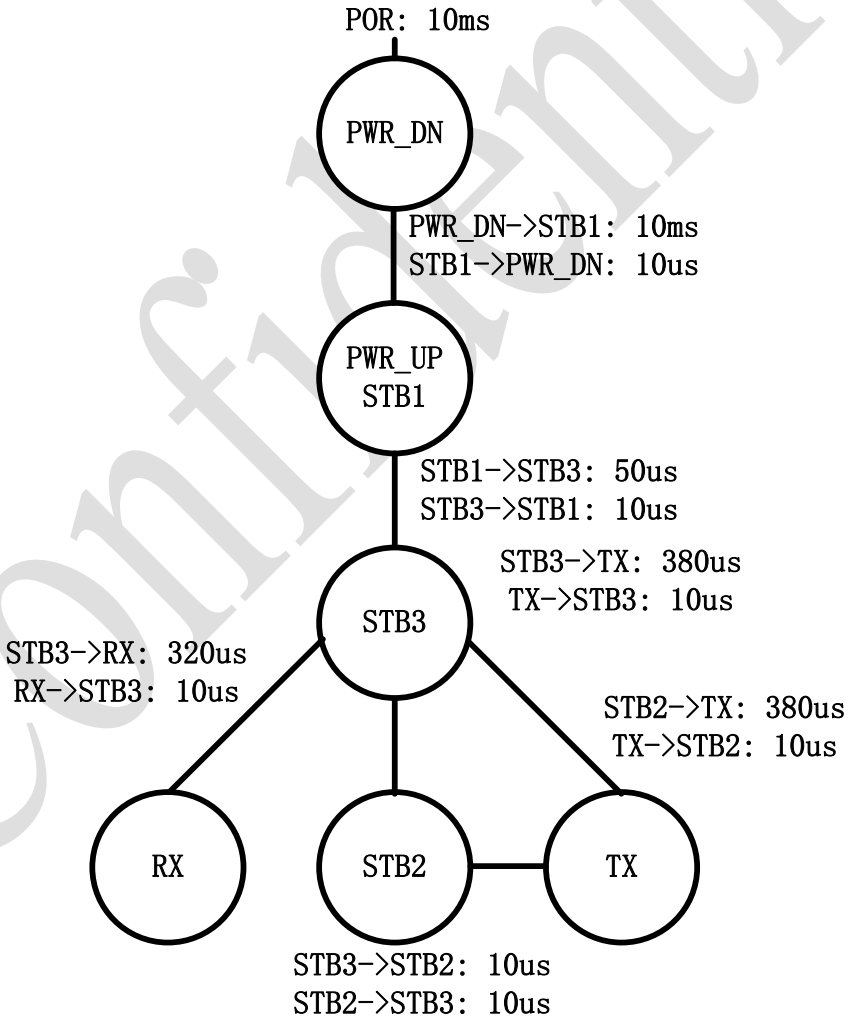

Figure 4-1 State diagram

4.2 Operational Modes Configuration

The Table 4-1 describes how to configure the operational modes and the functions.

Table 4-1 XN297L operational modes

MODE		PWR_DN	STB1	STB3	STB2	RX	TX
CONTROL BIT	PWR_UP	0	1	1	1	1	1
	EN_PM	0	0	1	1	1	1
	CE	0	0	0	1	1	1
	PRIM_RX	X	X	X	0	1	0
	FIFO state	X	X	X	TX FIFO empty	X	Data in TX FIFOs
FUNCTION DESCRIPTION	SPI Operation	√	√	√	√	√	√
	Keep Register Value	√	√	√	√	√	√
	Crystal Oscillator Work	X	√	√	√	√	√
	Crystal Oscillator Output	X	X	X	√	√	√
	Enable Power Management Module	X	X	√	√	√	√
	Enable TX Module	X	X	X	X	X	√
	Enable RX Module	X	X	X	X	√	X

4.3 Power Down Mode

In power down mode, all XN297L functions are turned off with a minimum current consumption. After entering power down mode, the XN297L stops working, but the contents of the registers remain unchanged. Power down mode is controlled by the PWR_UP bit in the register.

4.4 Standby-I Mode (STB1)

In standby-I mode, the chip maintains crystal oscillation but does not output to other modules. The other functional modules are turned off and the current consumption is small. The device enters to standby-I mode from power down mode by setting the PWR_UP bit in the CONFIG register to 1. In the transmit or receive mode, the chip can return to standby-I mode by setting the CE and EN_PM control signals to 0.

4.5 Standby-III Mode (STB3)

The device enters to standby- III mode from standby-I mode by setting the EN_PM bit to 1. The

standby mode-III is aimed to keep the chip's power management module precede the crystal output.

4.6 Standby-II Mode (STB2)

The standby-II mode can usually be understood as a preliminary transmission mode. The device enters to standby- II mode by setting the CE to 1 while the TX FIFO register is empty. At this time, the crystal oscillator has a strong output drive capability and the power management module of the chip is turned on. In standby-II mode, if a data packet is sent to the TX FIFO, the internal phase-locked loop (PLL) of the chip starts working immediately and after a lock time of the PLL, the transmitter transmits the data packet.

4.7 RX Mode

The device enters to RX mode by setting the PWR_UP, PRIM-RX, EN_PM and CE to 1. In RX mode, the RF part receives the signal from the antenna, then amplifies, downconverts, filters and demodulates it.The packe's validity will be judged according to the address, check code, data length, etc. The valid pakege will be uploaded to the RX FIFO and trigger interruption. If the RX FIFO is full, the received packet will be discarded.

4.8 TX Mode

The device enters to TX mode by setting the PWR_UP, EN_PMCE and CE to 1 while have PRIM_RX bit setting low and a payload in the TX FIFO. The XN297L remains in TX mode until the packet is sent. After the transmission is completed, the device returns to the standby mode. The XN297L employs PLL open-loop transmission, and the data packet is sent in a single packet.

5 Data Communication Modes

The XN297L chip works with the MCU to complete the communication function. The link layer, such as data frame frame, checksum, address judgment, data whitening scrambling code, data re-transmission and ACK response, is processed internally by the chip and does not require MCU participation.

The XN297L chip can be configured as two different RX FIFO registers (32 bytes) or one RX FIFO register (64 bytes) (shared by six receive channels), two different TX FIFO registers (32 bytes) or one TX FIFO register (64 bytes). MCU can access FIFO registers in power down mode and standby mode.

The communication modes of XN297L can be classified into two kinds:

- Without automatic retransmission without ACK communication mode (Normal BURST), the transmitter can use commands such as W_TX_PAYLOAD, REUSE_TX_PL, etc.
- With automatic retransmission with ACK communication mode (Enhanced BURST), the transmitter can use commands such as W_TX_PAYLOAD, W_TX_PAYLOAD_NOACK, REUSE_TX_PL, etc. The receiver can use commands such as W_ACK_PAYLOAD, etc.

Table 5-1 Normal BURST

Communication Name	**Normal BURST**	
Communication Party	PTX	PRX
Feature	One Way Transmit	One Way Receive
Framing Method of Transmiting Data	I	None
Start Command REUSE_TX_PL	Re-Transmit the Previous Packet	None

Table 5-2 Enhanced BURST

Communication Name	**Enhanced BURST**	
Communication Party	PTX	PRX
Feature	After transmiting data, wait for receiving ACK	After receiving the data, send back ACK
Framing Method Of Transmiting Data	Send data framing mode II	Send back ACK framing mode III
PTX using the REUSE_TX_PL command	Re-Transmit The Previous Packet	Once receive a packet, send back ACK
PTX using the W_TX_PAYLOAD command PRX using the W_ACK_PAYLOAD command	After transmiting data, wait to receive ACK PAYLOAD	After receiving data, send back ACK PAYLOAD, framing mode II
PTX using the W_TX_PAYLOAD_NO_ACK command	Transmit data once, not waiting for ACK, framing mode II	Receive data, do not return ACK

5.1 Normal BURST

In normal mode, the sender fetches data from the TX FIFO register and sends it. After the transmission is completed, the interrupt is reported (interrupt needs to be cleared), and the TX FIFO register clears the data (the TX FIFO needs to be cleared), the receiver receives a valid address and data. The MCU is notified of the interrupt, and the MCU can then read the data from the RX FIFO register (the TX FIFO, RX FIFO and interrupt all need to be cleared).

In Normal BURST, (0X01) EN_AA register is set to 0X00, (0X04) SETUP_RETR register is set to 0X00, (0X1C) DYNPD register is set to 0X00, The lower 3 bits of the (0X1D)FEATURE register are set to 000.

5.2 Enhanced BURST

In the enhanced burst, the party that initiates the communication is called PTX (the primary originating terminal), and the party that receives the data and responds is called the PRX (the primary receiving terminal). After the PTX sends the data, it waits for the response signal, and the PRX returns the response signal after receiving the valid data. If the PTX does not receive an acknowledgement signal within the specified time, it automatically resends the data. The automatic retransmission and auto answer functions are included with the XN297L chip and do not require MCU participation.

PTX automatically transfers to the TX mode waiting response signal after transmitting data. If the correct response signal is not received within the specified time, the PTX will resend the same data packet until the acknowledge signal is received, or the number of transmissions exceeds the ARC value (SETUP_RETR register) to generate the MAX_RT interrupt. The PTX receives the acknowledgement signal, that is, the data has been successfully transmitted (PRX receives valid data).Then the data in the TX FIFO are cleared and a TX_DS interrupt is generated (the TX FIFO and RX FIFO need to be cleared, and the interrupt needs to be cleared).

Each time PRX receives a valid data packet, it will return an ACK response signal. If the data is new data (the PID value is different from the previous packet data), it will be saved to the RX FIFO, otherwise it will be discarded.

In enhanced mode, it is necessary to ensure that the TX address of the PTX (TX_ADDR), the RX address of channel 0 (such as RX_ADDR_P0), and the RX address of the PRX (such as RX_ADDR_P5) are the same. For Example: In Figure 5-3, PTX5 corresponds to the data channel 5 of PRX, and the address is set as follows:

- PTX5: TX_ADDR=0xC2C3C4C5C1
- PTX5: RX_ADDR_P0=0xC2C3C4C5C1
- RX: RX_ADDR_P5=0xC2C3C4C5C1

Enhanced burst has the following characteristics:

- Reduce MCU control and simplify software operation.

- Strong anti-interference ability, reduce packet loss caused by instantaneous co-channel interference in wireless transmission, and easier to develop frequency hopping algorithm.
- During the retransmission process, reduce the operation time of the MCU each time to write data to be sent through the SPI interface.

5.3 Enhanced TX Mode

1. CE is set to 0, the PRIM_RX bit of the CONFIG register is set to 0.
2. When transmitting data, the transmit address (TX_ADDR) and valid data (TX_PLD) are written to the address register and the TX FIFO in bytes via the SPI interface. When the CSN pin is low, data is written, the CSN pin is set to high again, and the data write operation completes.
3. CE is set to 1 from 0, the transmission is started (CE is kept 1 for more than 30us, the operation takes effect).
4. In automatic reply mode (SETUP_RETR register is not set to 0, ENAA_P 0 = 1), PTX automatically switches channel 0 to RX mode to wait for the reply signal immediately after sending the data. If an ACK response signal is received within the valid response time range, the data is considered to have been sent successfully, and the TX_DS position of the status register is 1 and the data in the TX FIFO is automatically cleared. If the response signal is not received within the set time range, the data is automatically retransmitted.
5. If the automatic transfer counter (ARC_CNT) overflows (exceed the set value), the MAX_RT bit of the status register is set and the data in the TX FIFO is not cleared. When MAX_RT or TX_DS is 1, the IRQ pin generates a low interrupt (the corresponding interrupt needs to be enabled). Interrupts can be reset by writing to the status register.
6. The packet loss counter (PLOS_CNT) is incremented by one each time the MAX_RT interrupt is generated. The automatic transmission counter ARC_CNT counts the number of times the data packet is retransmitted; the packet loss counter PLOS_CNT counts the number of data packets that have not been successfully transmitted when the maximum number of allowed transmission times is reached.
7. After the MAX_RT or TX_DS interrupt is generated, the system enters standby mode.

5.4 Enhanced RX Mode

1. When CE is set to 0, the PRIM_RX bit in the CONFIG register is set first. The channel ready to receive data must be enabled (EN_RXADDR register). All auto-answer functions for data channels operating in Enhanced BURST mode are enabled by the EN_AA register. The valid data width is set by the RX_PW_PX register.

2. RX mode is started by setting CE to 1.
3. After the preset waiting time, PRX starts to detect the wireless signal.
4. After receiving valid data packets, data is stored in RX_FIFO, and RX_DR bit is set to 1, resulting in an interruption. In the status register, the RX_P_NO bit shows which channel the data was received.
5. Automatic transmit ACK response signal.
6. If CE remains at 1, continue to enter receive mode, if CE is set to 0, enter standby mode-III.
7. The MCU reads the data through the SPI port at an appropriate rate.

5.5 Packet Identification in Enhanced BURST

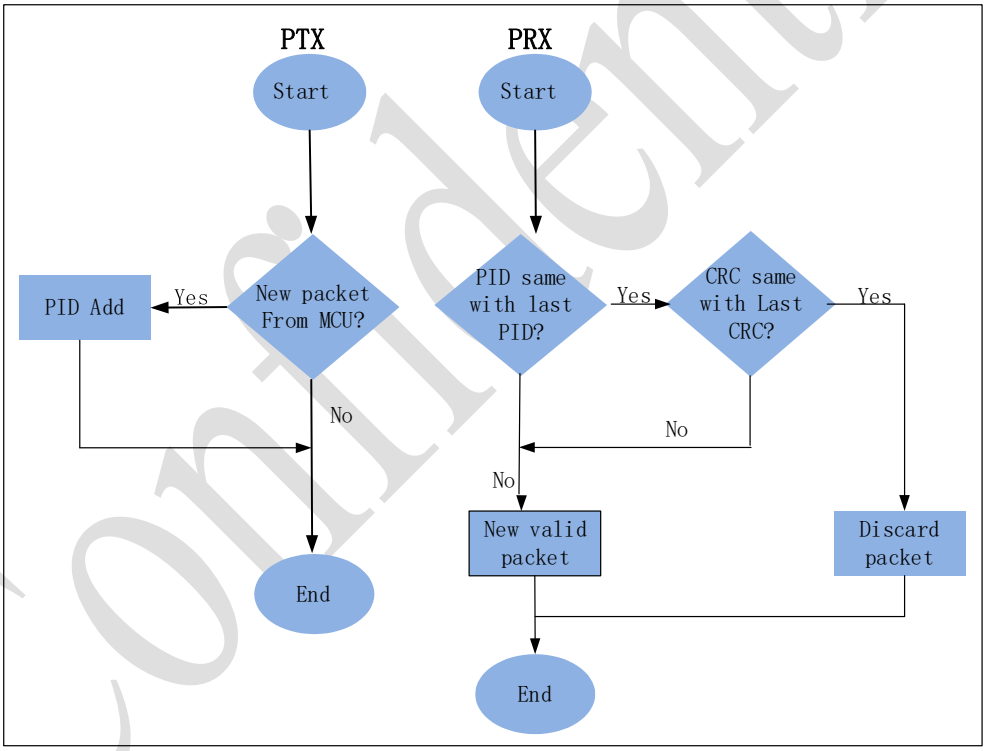

Figure 5-1 PID generation and detection

Each packet of data includes two PIDs (packet flag bits) to help the receiving terminal identify whether the data is new or retransmitted, preventing the same data packet from being stored multiple times. PID generation and detection is shown in Figure 5-1. The PID value adds 1 once the sender fetches a new packet from MCU.

5.6 The PTX and PRX Timing of Enhanced BURST

Figure 5-2 shows the internal timing diagram of the PTX and PRX communication. To make the communication successful must meet the following two conditions.

- Condition 1: The three periods sum of PTX (or PRX) transmit PLL stabilization + power amplifier enable + PLL open-loop is greater than the PLL stability time received by PRX (or PTX) 20us or more, thus ensuring that the time period in which the PTX (or PRX) transmits data is within the time period during which the PRX (or PTX) receives the data. That is:

  EX_PA_TIME + TX_SETUP_TIME + TRX_TIME > RX_SETUP_TIME +20us

- Condition 2: The four periods sum of PRX transmit ACK PLL stabilization + power amplifier enable + PLL open-loop+ transmiting ACK is less than the two periods sum of PTX receive PLL stabilization + wait ACK 20us or more, thus ensuring that the time period in which the PRX replies ACK is within the time period during which the PTX waits ACK. That is:

  EX_PA_TIME + TX_SETUP_TIME + TRX_TIME + SEND_ACK_TIME <

  RX_SETUP_TIME + RX_ACK_TIME - 80us

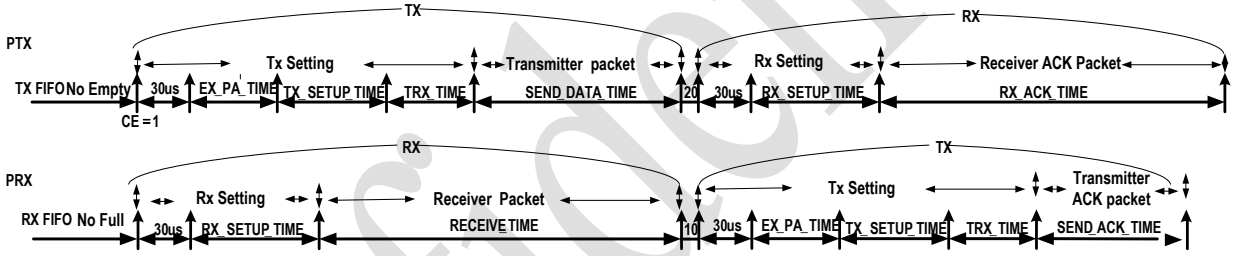

Figure 5-2 The timing of Enhanced BURST

5.7 One-To-Multi Communication at the Receiving End in Enhanced BURST

When the XN297L chip acts as a transmit terminal, different addresses can be used to communicate with multiple receiving eterminal for one-to-multi communication.

When the XN297L chip acts as a receive terminal, the XN297L chip can receive 6 channels of transmitter data with different addresses and the same frequency. Each data channel has its own address.

Which data channels are enabled are set by the register EN_RXADDR. The address of each data channel is configured by the register RX_ADDR_PX. Normally different data channels are not allowed to set the exact same address. As shown below, Table 5-3 gives an example of a multi-receive channel address configuration.

Table 5-3 Multi-channel address configuration

	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Data pipe 0(RX_ADDR_P0)	0xF1	0xD2	0xE6	0xA2	0x33
Data pipe 1(RX_ADDR_P1)	0xD3	0xD3	0xD3	0xD3	0xD3
Data pipe 2(RX_ADDR_P2)	0xD3	0xD3	0xD3	0xD3	0xD4
Data pipe 3(RX_ADDR_P3)	0xD3	0xD3	0xD3	0xD3	0xD5
Data pipe 4(RX_ADDR_P4)	0xD3	0xD3	0xD3	0xD3	0xD6
Data pipe 5(RX_ADDR_P5)	0xD3	0xD3	0xD3	0xD3	0xD7

It can be seen from Table 5-3 that the whole 40 bits addresses of 5 byte of data channel 0 are configurable, the address of data channel 1~5 is configured as 32-bit shared address (shared with data channel 1) + 8 bits of respective address (Lowest byte).

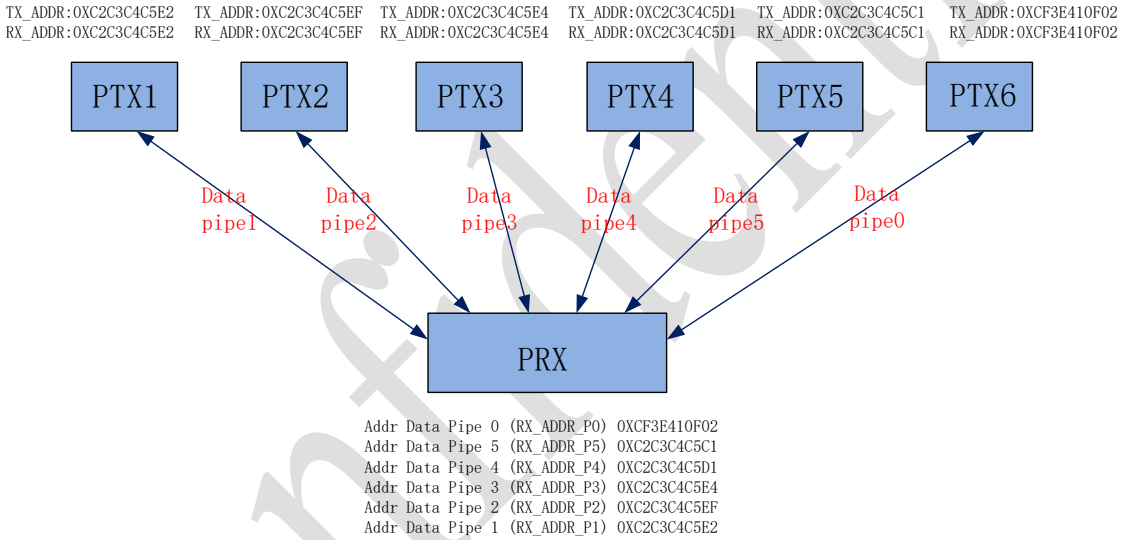

Figure 5-3 Example of data pipe addressing in star network

The XN297L chip can communicate with up to six different channels in RX mode, as shown in Figure 5-3. Each data channel uses a different address and shares the same channel. All transmitters and receivers are set to enhanced burst mode.

After receiving the valid data, the PRX records the TX address of the PTX and sends a response signal with the address as the target address. When PTX data channel 0 is used as the receive acknowledge signal, the RX address of data channel 0 is equal to the TX address to ensure that the correct acknowledge signal is received. Figure 5-3 shows an example of how PTX and PRX addresses are configured.

5.8 Data FIFO

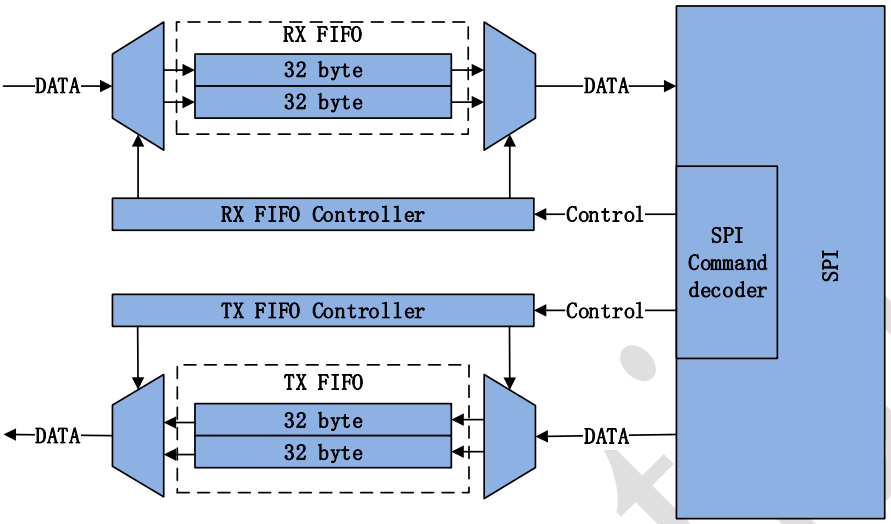

Figure 5-4 FIFO diagram

The XN297L contains the TX_FIFO and RX_FIFO. The FIFO can be read and written by the SPI command. The TX_FIFO is written by the W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK instructions in TX mode. If a MAX_RT interrupt is generated, the data in the TX_FIFO will not be cleared. In the RX mode, the payload in the RX_FIFO is read by the R_RX_PAYLOAD instruction, and the length of the payload is read by the R_RX_PL_WID instruction. The FIFO_STATUS register indicates the status of the FIFO.

5.9 Interrupt Pin

The interrupt pin (IRQ) of the XN297L chip is low-level triggered, the IRQ pin is initially high. When the TX_DS, RX_DR or MAX_RT in the status register is 1, and the corresponding interrupt reporting enable bit is 0, the interrupt of the IRQ pin is triggered. When the MCU writes '1' to the corresponding interrupt source, the interrupt is cleared. The IRQ pin interrupt trigger can be masked or enabled. By setting the interrupt report enable bit to 1, the interrupt trigger on the IRQ pin is disabled.

6 Packet format description

6.1 Packet Format for Normal BURST

The normal burst mode packet format is shown in Table 6-1, framing mode I.

In the address and data part of Table 6-1, the scrambling mode can be selected, according to the enable/disable scrambling code configuration bit.

Table 6-1 Packet format for Normal BURST

Preamble (3 bytes)	Address (3~5 bytes)	Payload (1~32/64 bytes)	CRC (0/2 bytes)

6.2 Packet Format for Enhanced BURST

The enhanced burst mode packet format is shown in Table 6-2, framing mode II.

In the address, identification and data part of Table 6-2, the scrambling mode can be selected, according to the enable/disable scrambling code configuration bit.

Table 6-2 Packet format for Enhanced BURST

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			Payload (0~32/64 byte)	CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)		

6.3 ACK Packet Format for Enhanced BURST

The ACK Packet format for Enhanced BURST is shown in Table 6-3, framing mode III.

The address and identification part of Table 6-3 need to select the same enable/disable scrambling mode as PTX.

Table 6-3 ACK Packet format for Enhanced BURST

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)	

6.4 Description of Packet Components

6.4.1 Preamble

The length of preamble in the XN297L is 3 bytes. The bit sequence of preamble is fixed. It can't be configured by the register. The preamble is used to synchronize the receiver demodulator to the incoming bit stream.

6.4.2 Address

The width of address can be configured in the AW register to be 3, 4 or 5 bytes. The receiver demodulate packet from the transmitter, if the address of packet is as same as the address of receiver, it will save the following payload in RX FIFO, otherwise discard the following payload and resume synchronization.

6.4.3 Packet Control Field

Packet control field is composed of 10bit, which contains a 7 bit payload length field, a 2 bit PID (Packet Identity) field and a 1 bit NO_ACK flag. And it only exists in enhanced BURST mode.

6.4.3.1 Payload Length identification

The 7 bit payload length filed specifies the length of payload in bytes. The length of payload can be 0 to 64 bytes.

Coding: 0000000= 0 byte (only used in empty ACK packets.) 1000000=64 bytes.

This field is only used if the Dynamic Payload Length function is enabled.

6.4.3.2 NO_ACK identification

The NO_ACK flag is only used when the XN297L is in enhanced burst mode. When using this function, the PTX goes directly to standby mode after sending a packet. PRX does not send ACK packets when it receives a packet.

6.4.4 Payload

The payload can be 0 to 64 bytes wide, which contains the user defined information.

In normal BURST mode, transmitter and receiver have the same static length. It is different between normal BURST mode and enhanced BURST mode, the enhanced BURST mode have dynamic payload length, expect for static payload length.

With the static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by RX_PW_Px registers on the receiver side. On the transmitter the payload length is set by the number of bytes clocked into the TX_FIFO and must equal the value in

the RX_PW_Px register on the receiver side.

DPL enables the dynamic payload length. It means that the transmitter sends packets with variable payload length to the receiver. The MCU can read the length of the received payload by using the R_RX_PL_WID command instead of using the RX_PW_Px registers. In order to enable DPL, the EN_DPL bit in the FEATURE register must be enabled. In RX mode the DYNPD register must be set. A PTX that transmitter to a PRX with DPL enabled must have the DPL_P0 bit in DYNPD set.

6.4.5 CRC

The CRC is the mandatory error detection mechanism in the packet. It can be enabled and set the number of bytes in the CONFIG register. If the CRC is enabled, the receiver will check the CRC of received packet. If they are not the same, the receiver will discard date and not generate an interrupt. And if the CRC is disabled, the receiver will save data in the FIFO, when the address is the same.

7 SPI Control Interface

The XN297L chip reads and writes to each register through the SPI control interface. The XN297L chip acts as a slave. The data rate of the SPI interface generally depends on the interface speed of the MCU, and its maximum data transfer rate is 4 Mbps. In order to save power, in power down mode and standby-I mode, the maximum transfer rate of SPI is 1Mbps.

The SPI interface is a standard SPI interface, shown in the Table 7-1. The SPI interface can be simulated using the general I/O port of the MCU. When the CSN pin is 0, the SPI interface waits for an execution instruction. An instruction is executed once the CSN pin is changed from 1 to 0. The contents of the status register can be read by MISO after the CSN pin changes from 1 to 0.

Table 7-1 SPI interface

PIN	I/O direction	Function description
IRQ	Output	The signal is active low and controlled by three maskable interrupt sources
CE	Input	The signal is active high and used to activate the chip in RX or TX mode
CSN	Input	SPI Chip Select
SCK	Input	SPI Clock
MOSI	Input	SPI Slave Data Input
MISO	Output	SPI Slave Data Output

7.1 SPI Commands

The SPI commands are shown in Table 7-2. Every new commands must be started by a high to low transition on CNS. The serial shifting SPI commands is in the following format:

<Command word: MS Bit to LS Bit (one byte)>

<Data bytes: LS Byte to MS Byte, MS Bit in each byte first>

Table 7-2 SPI commands

Command	Command word (binary)	Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LS Byte first	Read command and status registers. AAAAA =5 bit Register Map Address.
W_REGISTER	001A AAAA	1 to 5 LS Byte first	Write command and status registers. AAAAA = 5 bit Register Map Address. Executable in power down or standby modes only.
R_RX_PAY-LOAD	0110 0001	1 to 32/64 LS Byte first	Read RX-payload. A read operation starts at byte 0. Payload is deleted from RX FIFO after it is read. Used in RX mode.
W_TX_PAY-LOAD	1010 0000	1 to 32/64 LS Byte first	Write TX-payload.

			A write operation starts at byte 0. Used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode.
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode.
REUSE_TX_PL	1110 0011	0	Used for a PTX device, reuse last transmitted payload. TX payload reuse is active until FLUSH_TX is executed. TX payload reuse must be deactivated during package transmission.
ACTIVATE DEACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: • R_RX_PL_WID • W_TX_PAYLOAD_NOACK • W_ACK_PAYLOAD This is executable in power down or standby modes only. This write command followed by data 0x8C deactivates the following features.
R_RX_PL_WID	0110 0000	0	Read RX-payload width for the top, R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD	1010 1PPP	1 to 64 LS Byte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum two ACK packet payloads can be pending. Payloads with same PIPE are handled using first in - first out principle.
W_TX_PAYLOAD_NOACK	1011 0000	1 to 32/64 LS Byte first	Write Payload to be transmitted, used in TX mode. Disable auto ACK on this specific packet.
CE_FSPI_ON	1111 1101	1	SPI command CE internal logic 1, use the command followed by the data 0x00.
CE_FSPI_OFF	1111 1100	1	SPI command CE internal logic 0, use the command followed by the data 0x00.
RST_FSPI_HOLD RST_FSPI_RELS	0101 0011	1	With the command followed by data 0x5A, makes the XN297L into reset and maintain. With the command followed by data 0xA5, release the XN297 reset and starts to work normally.
NOP	1111 1111	0	No operation.

The R_REGISTER and W_REGISTER commands can operate on single or multi-byte registers. When accessing multi-byte registers, first read or write the MS Bit of LS Byte. Terminate the writing before all bytes in a multi-byte register are written, then it leaves the unwritten MS Byte(s) unchanged. For example, the LS Byte of RX_ADDR_P0 can be modified by writing only one byte to

the RX_ADDR_P0 register. The content of the status register is always read to MISO after a high to low transition on CNS.

7.2 SPI Timing

SPI operation and timing is shown in Figure 7-1 to Figure 7-3.

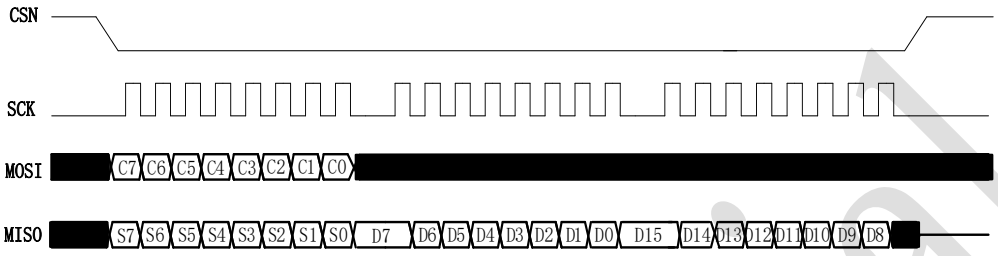

Figure 7-1 SPI read operation

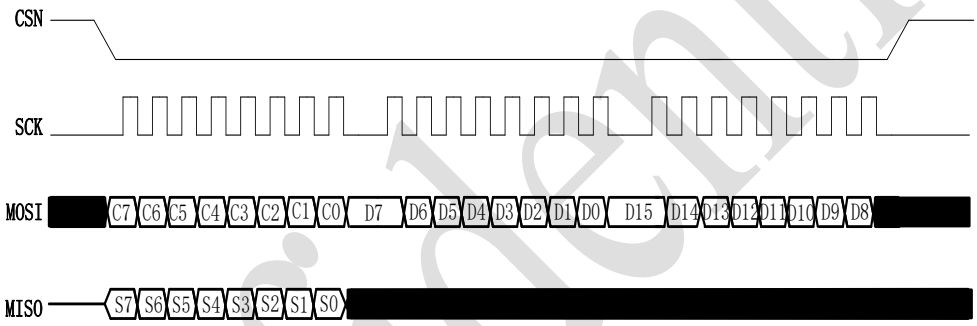

Figure 7-2 SPI write operation

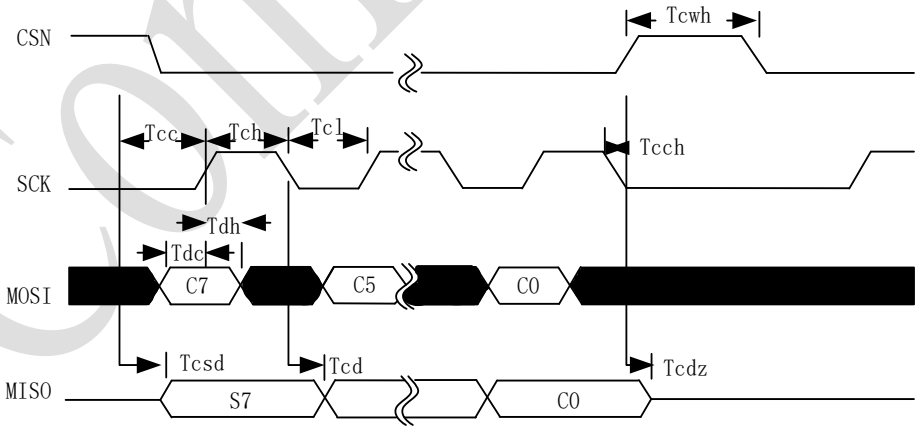

Figure 7-3 SPI NOP timing diagram

Table 7-3 SPI operation reference time

Symbol	Parameters	Min	Max	Units
Tdc	Data set-up time	15	-	ns
Tdh	Data hold time	2	-	ns
Tcsd	CSN signal effective time	-	40	ns
Tcd	SCK signal effective time	-	51	ns
Tcl	SCK signal low-level time	38	-	ns
Tch	SCK signal high-level time	38	-	ns
Fsck	SCK signal frequency	-	8	MHz
Tr,Tf	SCK signal rising/falling time	-	110	ns
Tcc	CSN set-up time	2	-	ns
Tcch	CSN hold time	2	-	ns
Tcwh	CSN invalid time	49	-	ns
Tcdz	CSN signal high impedance	-	40	ns

Note: The parameters of Table 7-3 can be adjusted according to the selected MCU.

Figure 7-1~ Figure 7-3 and Table 7-3 show the SPI operation and timing. The following symbols are used in the figure:

C_i - SPI instruction bit

S_i – State register bit

D_i – Data bit(Remarks: from low byte to high byte, the high bit in each byte is before)

Among: i=1, 2, 3……n.

7.3 SPI read/write mode

1）If there is a read command operation (including the three commands R_REGISTER, R_RX_PAYLOAD, and R_RX_PL_WID), the DATA pin will first be in the input state, and will automatically switch to the output state on the eighth clock falling edge of the SCK signal, and will output the signal on the subsequent clock rising edges. The GPIO corresponding to the DATA pin of the MCU is required to switch from the output state to the input state after the hold time of the eighth clock rising edge of the SCK signal.

2）CE_SEL needs to be set to 1 to start the command mode control. CE_L_sel sets to 1 to enable the weak pull-down resistor of the GPIO of CE. The CE state is controlled by using the CE_FSPI_ON/CE_FSPI_OFF command.

3）The interrupt status is obtained by querying the STATUS register.

4）In the transmission process, it is used to modify the necessary registers in STB1 or STB3 state first and write PAYLOAD, CE high 30us and then CE low, which makes it enter into the transmitting mode. Wait for the completion of sending (about 2ms) and then carry out SPI read/write operation. If the SPI read/write operation is performed during the transmission process, it will cause power ripple and affect the quality of the transmit signal.

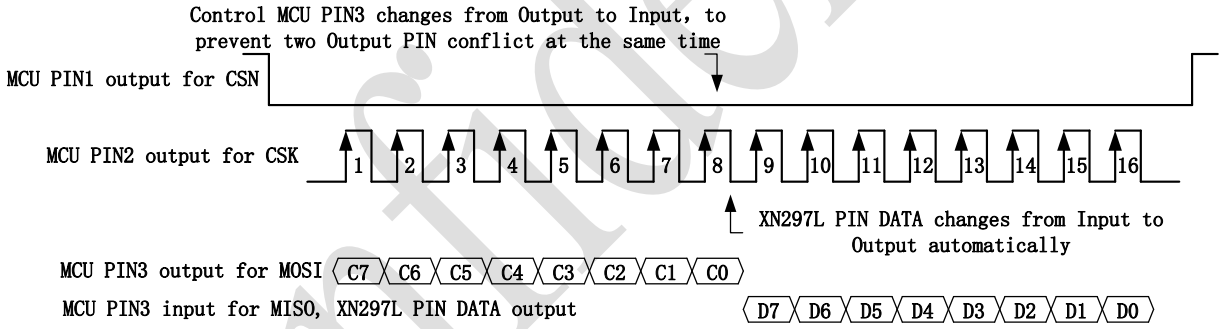

Figure 7-4 3-wire SPI read/write operation

8 Register Map

The XN297L can be configured and controlled by SPI reading/writing the registers shown in the Table 8-1.

Table 8-1 Register Map

Address（hex）	Mnemonic	Bit	Reset value	type	Description
00	CONFIG	-	-	-	Configuration register
	EN_PM	7	0	R/W	STB mode selection (Premise PWR_UP = 1): 1: Enter STB3 0: Enter STB1
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR: 1: Interrupt not reflected on the IRQ pin 0: Reflect RX_DR as active low interrupt on the IRQ pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS: 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT: 1: Interrupt not reflected on the IRQ pin 0: Reflect MAX_RT as active low interrupt on the IRQ pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high.
	N/A	2	0	R/W	CRC encoding scheme: '0' - 1 byte '1' – 2 bytes
	PWR_UP	1	0	R/W	1: POWER UP, 0:POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control: 1: PRX, 0: PTX
01	EN_AA Enhanced Burst	-	-	-	Enable ‘Auto Acknowledgment’ Function
	Reserved	7:6	00	R/W	Only 00 allowed
	ENAA_P5	5	0	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	0	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	0	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	0	R/W	Enable auto acknowledgement data pipe 2
	ENAA_P1	1	0	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0
02	EN_RXADDR	-	-	-	Enabled RX Addresses

	Reserved	7:6	00	R/W	Only 00 allowed
	ERX_P5	5	0	R/W	Enable data pipe 5
	ERX_P4	4	0	R/W	Enable data pipe 4
	ERX_P3	3	0	R/W	Enable data pipe 3
	ERX_P2	2	0	R/W	Enable data pipe 2
	ERX_P1	1	0	R/W	Enable data pipe 1
	ERX_P0	0	1	R/W	Enable data pipe 0
03	SETUP_AW	-	-	-	Setup of Address Widths (common for all data pipes)
	Reserved	7:2	000000	R/W	Only 000000 allowed
	AW	1:0	11	R/W	RX/TX Address field width: '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' – 5 bytes LS Byte is used if address width is below 5
04	SETUP_RETR	-	-	-	Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Retransmit Delay: ‘0000’ – Wait 250µS ‘0001’ – Wait 500µS ‘0010’ – Wait 750µS …….. ‘1111’ – Wait 4000µS (Delay defined from end of transmission to start of next transmission)
	ARC	3:0	0011	R/W	Auto Retransmit Count: ‘0000’ –Re-Transmit disabled ‘0001’ – Up to 1 Re-Transmit on fail of AA …… ‘1111’ – Up to 15 Re-Transmit on fail of AA
05	RF_CH	-	-	-	RF Channel
	Reserved	7	0	R/W	Only 0 allowed
	RF_CH	6:0	1001110	R/W	Sets the frequency channel F0=2400+(RF_CH<6:0>
06	RF_SETUP	-	-	-	RF Setup Register
	RF_DR	7:6	00	R/W	Sets Data Rate: 01: 2Mbps 00: 1Mbps 11: 250kbps 10: Reserved
	RF_PWR	5:0	111111	R/W	Sets RF output power: 100111: 11dBm 010101: 9dBm

					101100: 5dBm 010100: 4dBm 101010: -1dBm 011001: -10dBm 110000:-23dBm
07	STATUS	-	-	-	Status Register
	Reserved	7	0	R/W	Only 0 allowed
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO. Write 1 to clear bit.
	TX_DS	5	0	R/W	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit.
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO: 000-101: Data Pipe Number 110: Not Used 111: RX FIFO Empty
	TX_FULL	0	0	R	TX FIFO full flag: 1: TX FIFO full 0: Available locations in TX FIFO
08	OBSERVE_TX	-	-	-	Transmit observe register
	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH.
	ARC_CNT	3:0	0	R	Count retransmitted packets. The counter is reset when transmission of a new packet starts.
09*	DATAOUT	7:0	-	-	Received Power Detector RSSI<3:0>
	RSSI_RT	7:4	0000	R	The value of RSSI for real time
	RSSI_SY	3:0	0000	R	The value of RSSI after Synchronize
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0.5 Bytes maximum length. (LS Byte is written first. Write the number of bytes defined by SETUP_AW).

0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LS Byte is written first. Write the number of bytes defined by SETUP_AW).
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2. Only LSB. MS Bytes are equal to RX_ADDR_P1[39:8].
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3. Only LSB. MS Bytes are equal to RX_ADDR_P1[39:8].
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4. Only LSB. MS Bytes are equal to RX_ADDR_P1[39:8].
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5. Only LSB. MS Bytes are equal to RX_ADDR_P1[39:8].
10	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	Transmit address. Used for a PTX device only. (LS Byte is written first) set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device with enhanced ShockBurst™.
11	RX_PW_P0	-	-	-	-
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P0	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 0 (1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
12	RX_PW_P1	-	-	-	-
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P1	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 1 (1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
13	RX_PW_P2	-	-	-	-
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P2	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 2 (1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes

					64 = 64 bytes
14	RX_PW_P3	-	-	-	-
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P3	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 3 (1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
15	RX_PW_P4	-	-	-	-
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P4	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 4(1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
16	RX_PW_P5	-	-	-	-
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P5	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 5 (1 to 64 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes 64 = 64 bytes
17	FIFO_STATUS	-	-	-	FIFO Status Register
	N/A	7	0	R	Only 0 allowed
	TX_REUSE	6	0	R	Used for a PTX device Pulse the rfce high for at least 10μs to Reuse last transmitted payload. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI commands W_TX_PAYLOAD or FLUSH TX.
	TX_FULL	5	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
	TX_EMPTY	4	1	R	TX FIFO empty flag: 1: TX FIFO empty 0: Data in TX FIFO

	N/A	3	0	R	Only '00' allowed
	N/A	2	0	R	RX FIFO full flag: 1: RX FIFO full 0: Available locations in RX FIFO
	RX_FULL	1	0	R	RX FIFO empty flag: 1: RX FIFO empty 0: Data in RX FIFO
	RX_EMPTY	0	1	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
N/A	TX_PLD	255:0	X	W	Written by separate SPI command TX data payload register 1-32 or64 bytes. This register is implemented as a FIFO with two levels 32 bytes or one levels 64 bytes. Used in TX mode only.
N/A	RX_PLD	255:0	X	R	Read by separate SPI command RX data payload register 1-32 or64 bytes. This register is implemented as a FIFO with two levels 32 bytes or one levels 64 bytes. All RX channels share the same FIFO.
19*	DEMOD_CAL	7:0	-	-	Special Function Register
1A*	RF_CAL2	47:0	-	-	Special Function Register
1B*	DEM_CAL2	23:0	-	-	Special Function Register
1C	DYNPD	-	-	-	Enable dynamic payload length
	Reserved	7:6	00	R/W	Only 00 allowed
	DPL_P5	5	0	R/W	Enable dynamic payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable dynamic payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable dynamic payload length data pipe 3. (Requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P0)
1D*	FEATURE	7:0	-	R/W	Feature Register
	Reserved	7	0	R/W	Only 00 allowed
	MUX_PA_IRQ	6	0	R/W	The IRQ pin output: 0: IRQ signal 1: EN_PA signal
	CE_SEL	5	0	R/W	CE control: 0: CE is controlled by the pin

					1: CE is controlled by SPI command
	DATA_LEN_SEL	4:3	00	R/W	FIFO length: 11: 64byte 00: 32byte
	EN_DPL	2	0	R/W	Enable Dynamic Payload Length
	EN_ACK_PAY	1	0	R/W	Enable Payload with ACK
	EN_NOACK	0	0	R/W	Enable the W_TX_PAYLOAD_NOACK command
1E*	RF_CAL	23:0	-	R/W	Special Function Register
1F*	BB_CAL	-	-	R/W	Special Function Register
	Reserved	39:32	01000110	R/W	Only 0X01000110 allowed
	INVERTER	31	1	R/W	Whether to reverse the RX path data before entering RX Block: 1: reverse 0: remain unchanged
	DAC_MODE	30	0	R/W	The format of dac_out[5:0] for DAC input: 1: dac_out[5:0]<= [0:5] 0: dac_out[5:0]<= [5:0]
	DAC_BASAL	29:24	011100	R/W	The initial offset of DAC input.
	TRX_TIME	23:21	011	R/W	The time from sending carrier to sending data packet, the length of time can be calculated as the following formula: TRX_TIME × 8 + 7.5, the unit is us.
	EX_PA_TIME	20:16	00111	R/W	The time from TX PLL enable to PA enable, the length of time can be calculated as the following formula: EX_PA_TIME×16, the unit is us.
	TX_SETUP_TIME	15:11	01101	R/W	The time from PA enable to TX PLL Open, the length of time can be calculated as the following formula: TX_SETUP_TIME×16, the unit is us.
	RX_SETUP_TIME	10:6	10100	R/W	The time from RX PLL enable to RX enable, the length of time can be calculated as the following formula: RX_SETUP_TIME×16, the unit is us.
	RX_ACK_TIME	5:0	001010	R/W	The time from entering RX mode to waiting ACK, the length of time is different for different data rate. For 2Mbps data rata, the length of time can be calculated as the following formula: RX_ACK_TIME×16, the unit is us. For 1Mbps data rata, the length of time can be calculated as the following formula:

					RX_ACK_TIME×32, the unit is us. For 250Kbps data rata, the length of time can be calculated as the following formula: RX_ACK_TIME×128, the unit is us.

Note: Special function registers are declared in the software design reference.

9 Application Reference Design

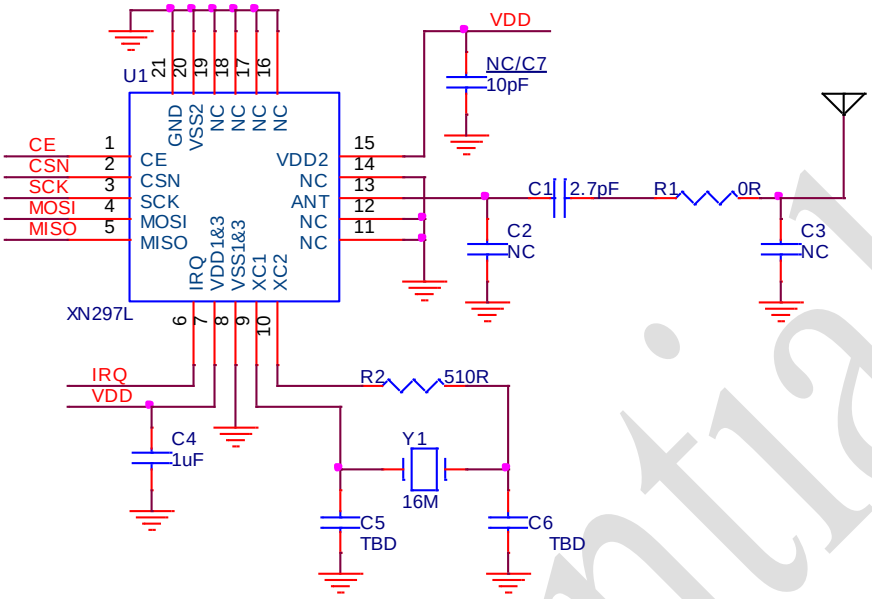

Figure 9-1 The XN297L schematic for package of QFN20 3*3

Note 1: NC pin can be floating.

Note 2: R1, C2 and C3 are used for output spectrum spurious filtering, they can be omitted if no need to meet RF regulatory standards.

Note 3: The XC2 pin is connected with a 510 ohm resistor to ensure that all types of crystal oscillator can be normally operated.

Note 4: The recommended value of C5 and C6 is 15~36 pF, depending to crystal load capacitance.

Note 5: C7 can be NC.

Note 6: The recommended value of C1 is 4~10 pf.

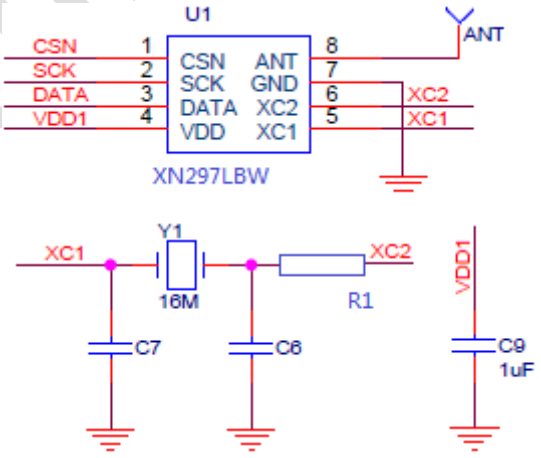

Figure 9-2 The XN297L schematic for package of SOP8

Note 1: The notice of the XN297L schematic for package of QFN20 pin 3×3 is also applicable for SOP8 package.

10 Package Dimensions

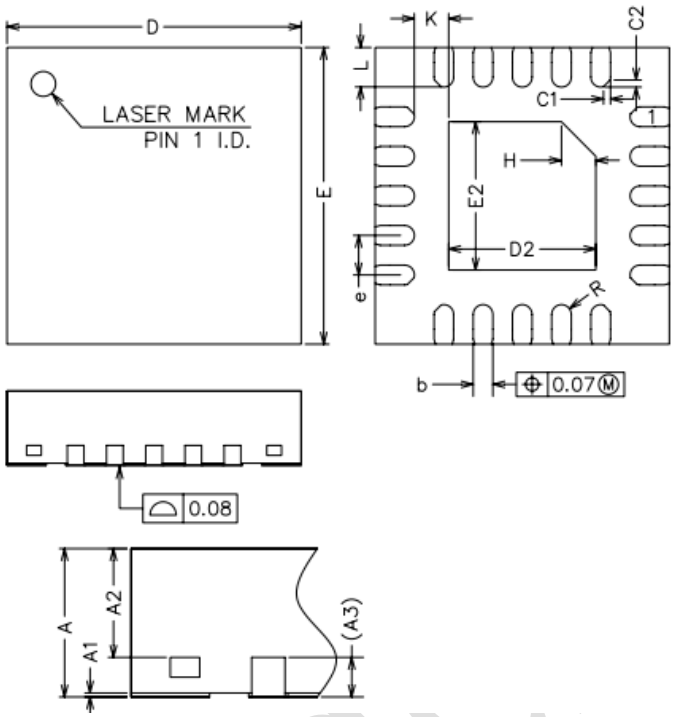

Figure 10-1 Top view, bottom view and side view of XN297L for the QFN20 3×3 package

Table 10-1 Package detail parameters for the QFN20 pin 3×3 package

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20RF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e	0.30	0.40	0.50
H	0.35REF		
K	0.35REF		
L	0.35	0.40	0.45
R	0.085	-	-
C1	-	0.07	-
C2	-	0.07	-

Note 1: Units of measure is millimeter（Same below）.

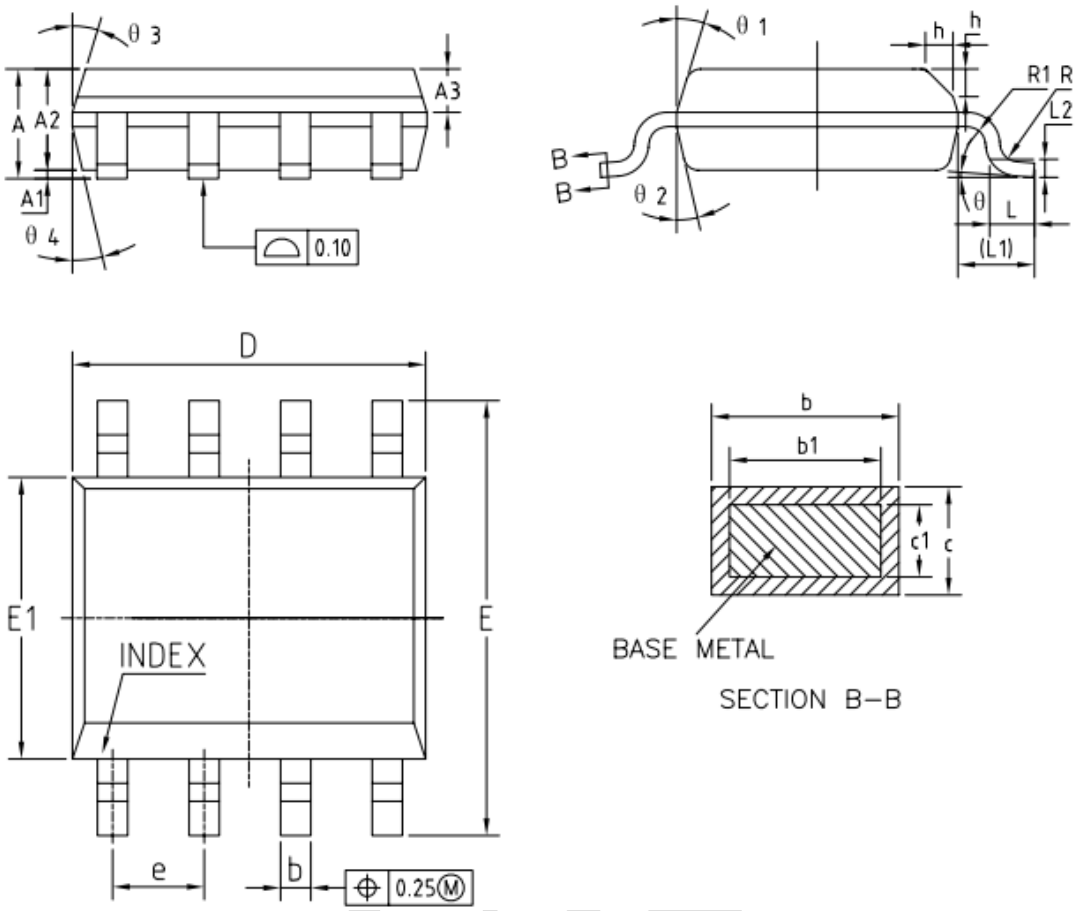

Figure 10-2 XN297L SOP8 package

Table 10-2 Package detail parameters for the SOP8 package

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	-	-
R1	0.07	-	-

h	0.30	0.40	0.50
Ø	0°	-	8°
Ø1	15°	17°	19°
Ø2	11°	13°	15°
Ø3	15°	17°	19°
Ø4	11°	13°	15°

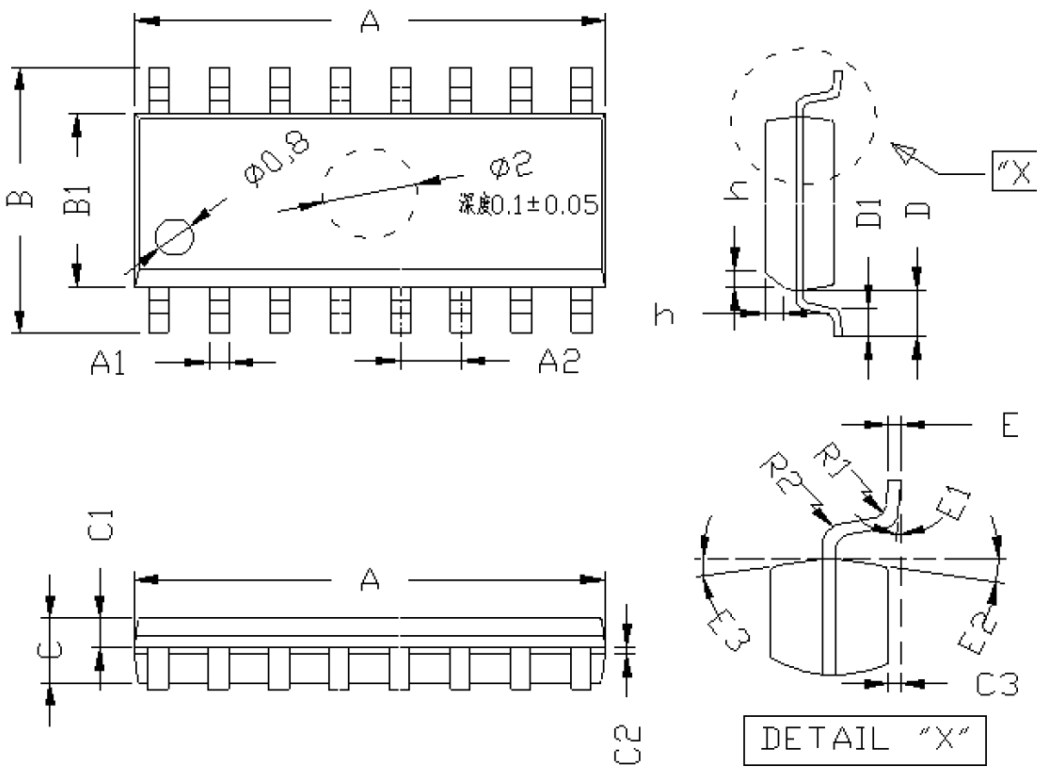

Figure 10-3 XN297L SOP16 package

Table 10-3 Package detail parameters for the SOP16 package

SYMBOL	MIN	NOM	MAX
A	9.80	9.90	10.00
A1	0.36	0.43	0.51
A2	1.27BSC		
B	5.80	6.00	6.20
B1	3.80	3.90	4.00
C	1.25	1.45	1.55
C1	0.55	0.65	0.75
C2	0.19	0.20	0.21
C3	0.05	0.10	0.15
D	1.04REF		

D1	0.52	0.62	0.72
E	0.25BSC		
E1	0°	4°	8°
E2	6°	8°	10°
E3	6°	8°	10°
R1	0.07TYP		
R2	0.07TYP		
h	0.30	0.40	0.50