Panchip Microelectronics Co., Ltd.

PAN2025

Datasheet

2.4GHz RF Transceiver SOC

Version: 1.3

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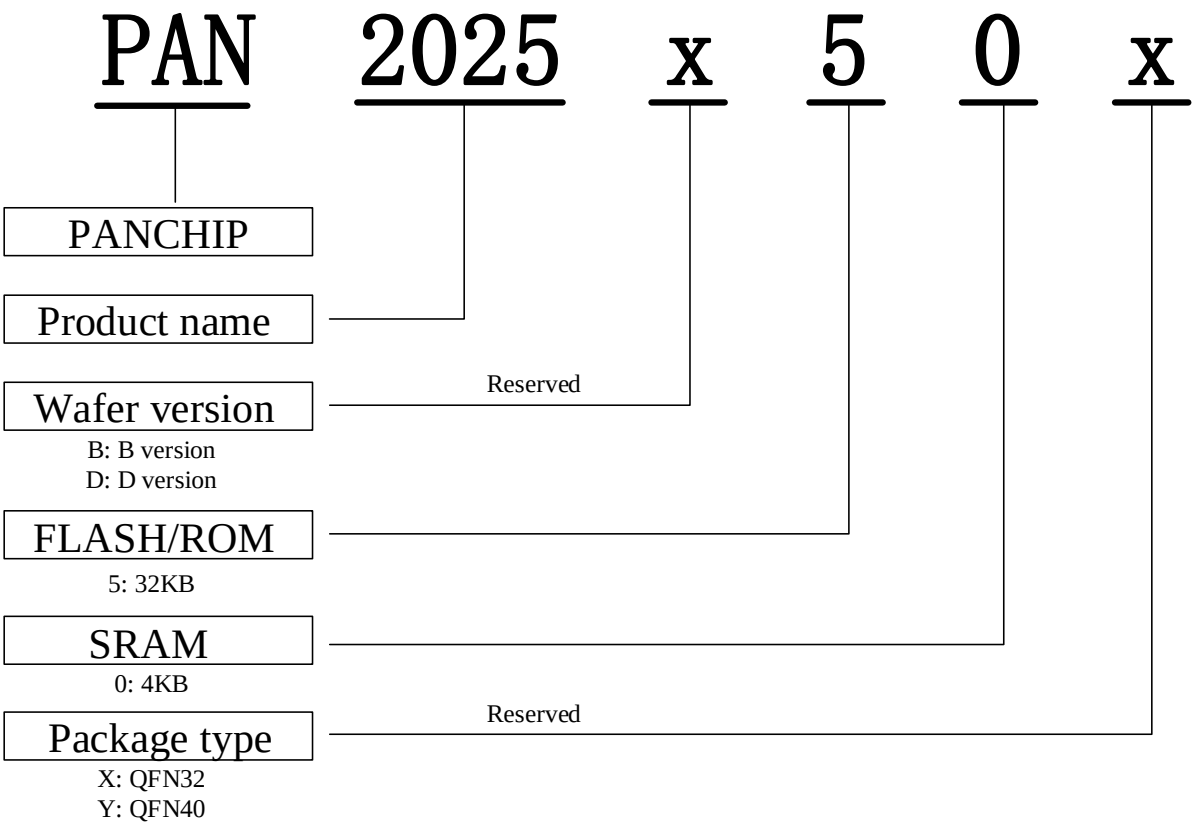
REVISION HISTORY

Version	Date	Content	Reference
1.0	Nov.2019	Initial	-
1.1	Feb.2020	Refresh: ● The value of voltage to 2.2~3.6V ● Part of the register description	-
1.2	Aug.2020	Refresh: Refresh to D version. Refresh the voltage range of ADC.	-
1.3	Jan.2021	Refresh: ● The application reference diagram	-

Naming Rules



Product Series

Product series	Wafer version[Note2]	MCU	Flash	SRAM	Package	Timer	PWM	ADC[Note1]	I/O	Connectivity		
										UART	I2C	SPI
PAN2025B50X	B	72 MHz	32 KB	4 KB	QFN32	2×32bits	8	7ch 12bits	21	4	1	1
PAN2025B50Y	B	72 MHz	32 KB	4 KB	QFN40	2×32bits	8	8ch 12bits	24	4	1	1
PAN2025D50X	D	72 MHz	32 KB	4 KB	QFN32	2×32bits	8	7ch 12bits	21	4	1	1
PAN2025D50Y	D	72 MHz	32 KB	4 KB	QFN40	2×32bits	8	8ch 12bits	24	4	1	1

The main difference between PAN2025B and PAN2025D are shown as follow:

Note 1: Analog input voltage range: 0~2V or 0~VDD for PAN2025BX and PAN2025BY.

Analog input voltage range: 0~2V or 0~(VDD-0.7) for PAN2025DX and PAN2025DY.

Note 2: RF communication mode: PAN2025B is recommended to communicate in RX mode. PAN2025D can communicate both in TX and RX mode.

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Abbreviation

ADC	Analog-to-Digital Converter
APROM	Application ROM
BOD	Brown-Out Detector
DPLL	Digital Phase Locked Loop
DSSS	Direct Sequence Spread Spectrum
ESD	Electro-Static Discharge
GFSK	Gauss Frequency Shift Keying
GPIO	General-Purpose Input/Output
I2C	Inter-Integrated Circuit
ISM	Industrial Scientific Medical
ISP	In-System Programming
LDO	Low Dropout Regulator
LDROM	Loader ROM
LVR	Low Voltage Reset
MCU	Microcontroller Unit
PWM	Pulse Width Modulation
RF	Radio Frequency
RSSI	Received Signal Strength Indication
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transmitter
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

1 General Description

The PAN2025 is a system-on-chip (SOC), embedded with 2.4GHz radio frequency(RF) transceiver and 32-bit microcontroller unit(MCU). The 2.4GHz transceiver is designed to operate in the world-wide ISM frequency band at 2.400~2.483GHz. It integrates radio RF transceiver, frequency synthesizer, crystal oscillator, baseband GFSK and DSSS modem, and other related modules. The PAN2025 supports both one-to-one and one-to-multiple communication with ACK. TX power, frequency channel, and data rates are configurable. Matching network and other external components are integrated into the chip to reduce the system cost.

The 32-bit MCU supports a wide range of applications from low-end, price-sensitive designs to computing-intensive system.

The PAN2025 can run up to 72 MHz and operate at a wide voltage range of 2.2V ~ 3.6V and temperature range of -40℃~ +85℃. The embedded program flash size is up to 32K bytes and SRAM size is up to 4K bytes. It also offers configurable flash size for the ISP.

The PAN2025 has many high-performance peripherals, such as 16 MHz internal RC oscilla-tor (±1% accuracy after calibration), I/O port with up to 24 pins, three 32-bit timers, four UARTs, one SPI interface, one I2C interface, one 16-bit PWM generator providing eight channels, one 8-channel 12-bit ADC, Watchdog Timer, Window Watchdog Timer and one Brown-out Detector. All these peripherals have been integrated into the PAN2025 to reduce the number of com-ponents, board area and system cost.

Additionally,the PAN2025 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end products. PAN2025 also supports IAP (In-Application-Programming) function, users can switch the code execution without resetting the chip after the embedded flash is updated. There are two kinds of packages, QFN32 and QFN40, which are compatible with Panchip's PAN163 and PAN159 products respectively.

1.1 Key Features

- RF
  - Radio
    - Frequency band: 2.400~2.483GHz
    - Data rate: 2Mbps, 1Mbps
    - DSSS and GFSK modulation
    - RF communication mode: PAN2025B is recommended to communicate in RX mode. PAN2025D can communicate both in TX and RX mode.
  - Receiver
    - -100dBm sensitivity at 1Mbps@DSSS
    - -91dBm sensitivity at 1Mbps@GFSK
  - Transmitter
    - Programmable output power: 12, 10, 8, 7, 6, 5, 4, 3, 2, 1, 0 or -4dBm
    - 25mA at 0dBm output power
    - 55mA at 10dBm output power
- Core

- 32-bit MCU running up to 72 MHz
- One 24-bit system timer
- Supports three level low power mode
- One single-cycle 32-bit hardware multiplier
- Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints

- Built-in LDO for wide operating voltage: 2.2V to 3.6V
- Memory
  - Up to 29 KB internal flash memory for program memory (APROM)
  - Configurable flash memory for data memory (Data Flash)
  - 2 KB internal flash memory for loader (LDROM)
  - Up to 4 KB internal SRAM
- Low Power
  - Active mode RX:20mA
  - Active mode TX at 0dBm:25mA
  - Active mode TX at 10dBm:55mA
  - Standby mode (external interrupts, CPU Power Down):0.2uA
  - Standby mode (external interrupts, CPU Power Down, SRAM retention): 1uA
  - Standby mode (sleep timer running, CPU Power Down):2.5uA
  - Standby mode (sleep timer running, CPU Sleep, SRAM retention): 3.3uA
- Clock Control
  - Programmable system clock sources
  - 16 MHz external crystal oscillator
  - Built-in 16 MHz internal high speed RC oscillator
  - Built-in 32 KHz internal low speed RC oscillator
  - Internal DPLL allowing CPU frequency up to maximum 72 MHz
- I/O Port
  - Up to 24 general-purpose I/O (GPIO) pins
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Schmitt trigger input
- Timer
  - Provides three 32-bit timers: each timer includes one 8-bit pre-scaler counter and one 24-bit up-counter
    - Supports Event Counter mode
    - Supports Toggle Output mode
    - Supports external trigger in Pulse Width Measurement mode
    - Supports external trigger in Pulse Width Capture mode
- WDT
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- WWDT

  - Flexible WWDT time-out window period with 6-bit down-counter value and 6-bit compare value
  - Supports 4-bit value to program the prescale counter's period of WWDT counter, the prescale counter is up to 11 bits
- PWM
  - Up to four built-in 16-bit PWM generators, providing eight PWM outputs or four complementary pairs of PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-time generator for each PWM generator
- UART
  - Four UART devices
  - Buffered receiver and transmitter, each with 8-byte FIFO
  - Programmable baud-rate generator, baud rate up to 1 system clock
- SPI
  - One SPI device
  - Master frequency up to 24 MHz, and Slave frequency up to 10 MHz
  - Supports Master/Slave mode
  - Full-duplex synchronous serial data transfer
- I2C
  - One I2C devices
  - Supports Master/Slave mode
  - Bidirectional data transfer between Master and Slave
- ADC
  - Analog input voltage range: 0~2V or 0~VDD for PAN2025BX and PAN2025BY
  - Analog input voltage range: 0~2V or 0~(VDD-0.7) for PAN2025DX and PAN2025DY.
  - Guaranteed 12-bit resolution and 10-bit accuracy
  - Up to eight single-end analog input channels, one bandgap input channel, one RSSI input channel, one GND check channel and one voltage input channel.
- ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application-Programming) update
- BOD
  - With 4 programmable threshold levels: 3.0V/2.7V/2.4V/2.2V
  - Supports Brown-out interrupt and reset option
- 32-bit unique ID
- LVR
  - Threshold voltage level: 2.0±0.1V
- Operating Temperature: -40℃ ~85℃
- Operating Voltage: 2.2V ~ 3.6V
- Reliability:
  - ESD HBM pass ±5KV
  - ESD CDM pass ±2KV
  - ESD MM pass ±300V
- Packages:
  - QFN32 (5×5)
  - QFN40 (5×5)

1.2 Typical Applications

- Small flying saucer with four-axises rotor
- Remote control toys
- Smart home
- TV and set-top box remote control

2 Block Diagram

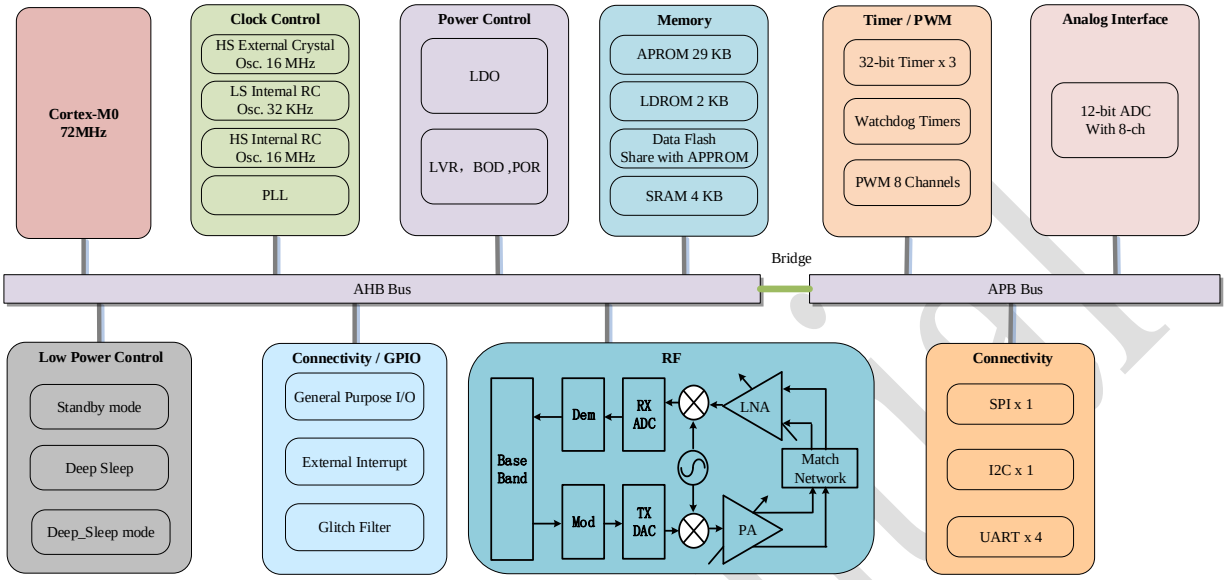

Figure 2-1 PAN2025 Block Diagram

3 Pin Information

3.1 QFN32-PIN

3.1.1 QFN32-Pin Diagram

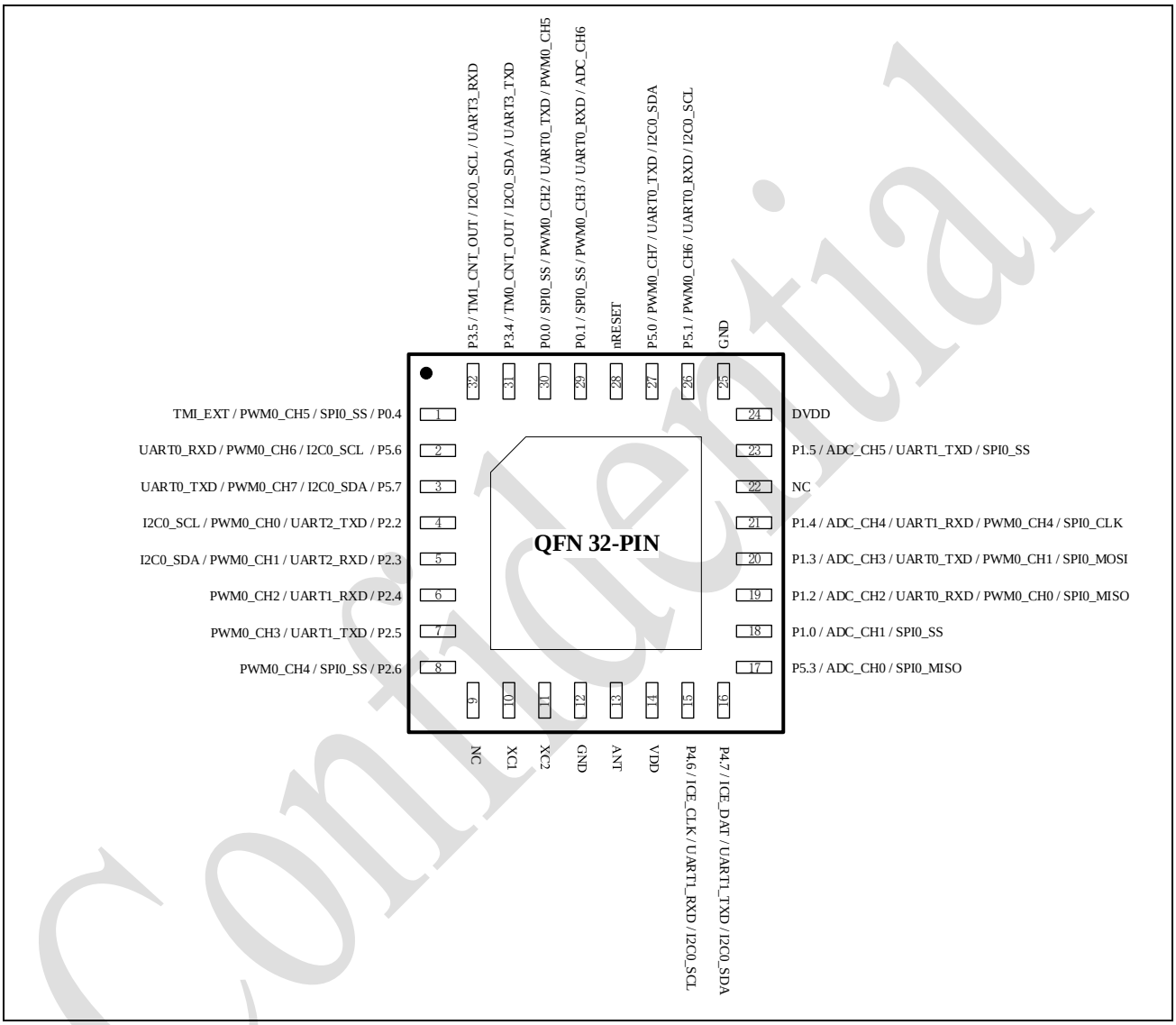

Figure 3-1 PAN2025 QFN 32-PIN Diagram

3.1.2 QFN32-Pin Description

Detail pin descriptions see Table 3-1.

Table 3-1 PAN2025 QFN32 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	P0.4	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin

	PWM0_CH5	O	PWM0 Channel5 Output Pin
	TM1_EXT	I	Timer1 External Input Pin
2	P5.6	I/O	General Purpose Digital I/O Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
	PWM0_CH6	O	PWM0 Channel6 Output Pin
	UART0_RXD	I	UART0 RX Pin
3	P5.7	I/O	General Purpose Digital I/O Pin
	I2C0_SDA	I/O	I2C0 Data Pin
	PWM0_CH7	O	PWM0 Channel7 Output Pin
	UART0_TXD	O	UART0 TX Pin
4	P2.2	I/O	General Purpose Digital I/O Pin
	UART2_TXD	O	UART2 TX Pin
	PWM0_CH0	O	PWM0 Channel0 Output Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
5	P2.3	I/O	General Purpose Digital I/O Pin
	UART2_RXD	I	UART2 RX Pin
	PWM0_CH1	O	PWM0 Channel1 Output Pin
	I2C0_SDA	I/O	I2C0 Data Pin
6	P2.4	I/O	General Purpose Digital I/O Pin
	UART1_RXD	I	UART1 RX Pin
	PWM0_CH2	O	PWM0 Channel2 Output Pin
7	P2.5	I/O	General Purpose Digital I/O Pin
	UART1_TXD	O	UART1 TX Pin
	PWM0_CH3	O	PWM0 Channel3 Output Pin
8	P2.6	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH4	O	PWM0 Channel4 Output Pin
9	-	-	-
10	XC1	AI	Crystal Pin1
11	XC2	AO	Crystal Pin2
12	GND	P	Ground Pin
13	ANT	AIO	Antenna Pin
14	VDD	P	SoC Power Supply VDD Pin
15	P4.6	I/O	General Purpose Digital I/O Pin
	ICE_CLK	I	ICE Clk Input Pin
	UART1_RXD	O	UART1 RX Pin
	I2C0_SCL	I/O	I2C0 CLK Pin

16	P4.7	I/O	General Purpose Digital I/O Pin
	ICE_DAT	I	Debug and Program Data Pin
	UART1_TXD	O	UART1 TX Pin
	I2C0_SDA	I/O	I2C0 Data Pin
17	P5.3	I/O	General Purpose Digital I/O Pin
	ADC_CH0	AI	ADC Channel0 Analog Input Pin
	SPI0_MISO	I	SPI0 MISO Pin
18	P1.0	I/O	General Purpose Digital I/O Pin
	ADC_CH1	AI	ADC Channel1 Analog Input Pin
	SPI0_SS	O	SPI0 SS Pin
19	P1.2	I/O	General Purpose Digital I/O Pin
	ADC_CH2	AI	ADC Channel2 Analog Input Pin
	UART0_RXD	I	UART0 RX Pin
	PWM0_CH0	O	PWM0 Channel0 Output Pin
	SPI0_MISO	I	SPI0 MISO Pin
20	P1.3	I/O	General Purpose Digital I/O Pin
	ADC_CH3	AI	ADC Channel3 Analog Input Pin
	UART0_TXD	O	UART0 TX Pin
	PWM0_CH1	O	PWM0 Channel1 Output Pin
	SPI0_MOSI	I	SPI0 MOSI Pin
21	P1.4	I/O	General Purpose Digital I/O Pin
	ADC_CH4	AI	ADC Channel4 Analog Input Pin
	UART1_RXD	I	UART1 RX Pin
	PWM0_CH4	O	PWM0 Channel4 Output Pin
	SPI0_CLK	O	SPI0 CLK Pin
22	-	-	-
23	P1.5	I/O	General Purpose Digital I/O Pin
	ADC_CH5	AI	ADC Channel5 Analog Input Pin
	UART1_TXD	O	UART1 TX Pin
	SPI0_SS	O	SPI0 SS Pin
24	DVDD	P	Core Power Supply, Generated by Internal LDO
25	GND	P	Ground Pin
26	P5.1	I/O	General Purpose Digital I/O Pin
	PWM0_CH6	O	PWM0 Channel6 Output Pin
	UART0_RXD	I	UART0 RX Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
27	P5.0	I/O	General Purpose Digital I/O Pin

	PWM0_CH7	O	PWM0 Channel7 Output Pin
	UART0_TXD	O	UART0 TX Pin
	I2C0_SDA	I/O	I2C0 Data Pin
28	nRESET	I	Reset Pin
29	P0.1	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH3	O	PWM0 Channel3 Output Pin
	UART0_RXD	I	UART0 RX Pin
	ADC_CH6	AI	ADC Channel6 Analog Input Pin
30	P0.0	I/O	General Purpose Digital I/O Pin
	PWM0_CH2	O	PWM0 Channel2 Output Pin
	UART0_TXD	O	UART0 TX Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH5	O	PWM0 Channel5 Output Pin
31	P3.4	I/O	General Purpose Digital I/O Pin
	TM0_CNT_OUT	O	TM0_CNT Output Pin
	I2C0_SDA	I/O	I2C0 Data Pin
	UART3_TXD	O	UART3 TX Pin
32	P3.5	I/O	General Purpose Digital I/O Pin
	TM1_CNT_OUT	O	TM1_CNT Output Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
	UART3_RXD	I	UART3 RX Pin
33	GND	P	Ground Pin

3.2 QFN40-PIN

3.2.1 QFN40-Pin Diagram

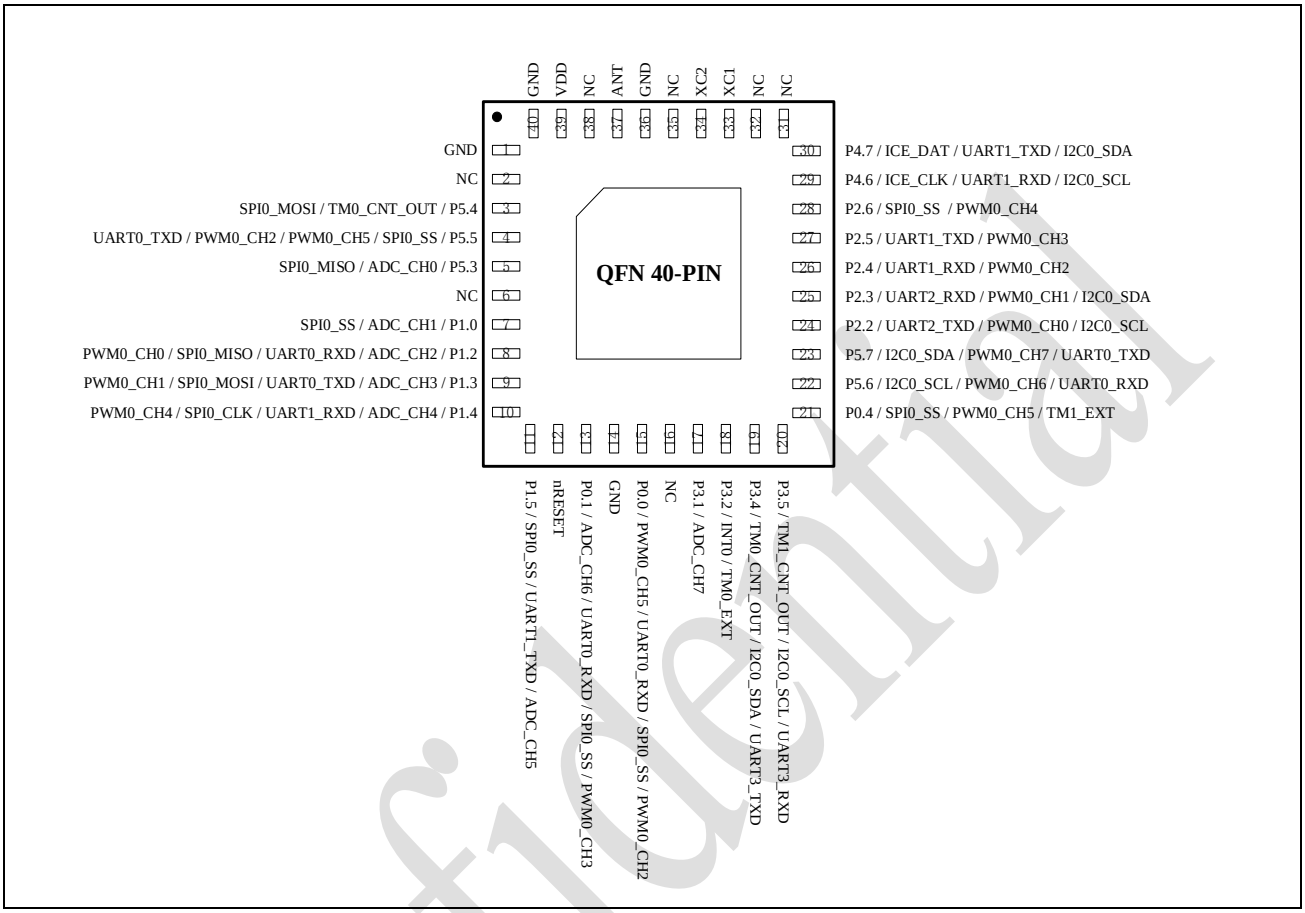

Figure 3-2 PAN2025 QFN 40-PIN Diagram

3.2.2 QFN40-Pin Description

Detail pin descriptions see Table 3-2.

Table 3-2 PAN2025 QFN40 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	GND	P	Ground Pin
2	-	-	-
3	P5.4	I/O	General Purpose Digital I/O Pin
	TM0_CNT_OUT	O	TM0_CNT Output Pin
	SPI0_MOSI	I	SPI0 MOSI Pin
4	P5.5	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH5	O	PWM0 Channel5 Output Pin
	PWM0_CH2	O	PWM0 Channel2 Output Pin

	UART0_TXD	O	UART0 TX Pin
5	P5.3	I/O	General Purpose Digital I/O Pin
	ADC_CH0	AI	ADC Channel0 Analog Input Pin
	SPI0_MISO	I	SPI0 MISO Pin
6	-	-	-
7	P1.0	I/O	General Purpose Digital I/O Pin
	ADC_CH1	AI	ADC Channel1 Analog Input Pin
	SPI0_SS	O	SPI0 SS Pin
8	P1.2	I/O	General Purpose Digital I/O Pin
	ADC_CH2	AI	ADC Channel2 Analog Input Pin
	UART0_RXD	I	UART0 RX Pin
	SPI0_MISO	O	SPI0 SS Pin
	PWM0_CH0	O	PWM0 Channel0 Output Pin
9	P1.3	I/O	General Purpose Digital I/O Pin
	ADC_CH3	AI	ADC Channel3 Analog Input Pin
	UART0_TXD	O	UART0 TX Pin
	SPI0_MOSI	I	SPI0 MOSI Pin
	PWM0_CH1	O	PWM0 Channel1 Output Pin
10	P1.4	I/O	General Purpose Digital I/O Pin
	ADC_CH4	AI	ADC Channel4 Analog Input Pin
	UART1_RXD	I	UART1 RX Pin
	SPI0_CLK	O	SPI0 CLK Pin
	PWM0_CH4	O	PWM0 Channel4 Output Pin
11	P1.5	I/O	General Purpose Digital I/O Pin
	ADC_CH5	AI	ADC Channel5 Analog Input Pin
	UART1_TXD	O	UART1 TX Pin
	SPI0_SS	O	SPI0 SS Pin
12	nRESET	I	Reset Pin
13	P0.1	I/O	General Purpose Digital I/O Pin
	ADC_CH6	AI	ADC Channel6 Analog Input Pin
	UART0_RXD	I	UART0 RX Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH3	O	PWM0 Channel3 Output Pin
14	GND	P	Ground Pin
15	P0.0	I/O	General Purpose Digital I/O Pin
	PWM0_CH5	O	PWM0 Channel5 Output Pin
	UART0_TXD	O	UART0 TX Pin

	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH2	O	PWM0 Channel2 Output Pin
16	-	-	-
17	P3.1	I/O	General Purpose Digital I/O Pin
	ADC_CH7	AI	ADC Channel7 Analog Input Pin
18	P3.2	I/O	General Purpose Digital I/O Pin
	INT0	I	External Interrupt0 Input Pin
	TM0_EXT	I	Timer0 External Input Pin
19	P3.4	I/O	General Purpose Digital I/O Pin
	TM0_CNT_OUT	O	TM0_CNT Output Pin
	I2C0_SDA	I/O	I2C0 Data Pin
	UART3_TXD	O	UART3 TX Pin
20	P3.5	I/O	General Purpose Digital I/O Pin
	TM1_CNT_OUT	O	TM1_CNT Output Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
	UART3_RXD	I	UART3 RX Pin
21	P0.4	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH5	O	PWM0 Channel5 Output Pin
	TM1_EXT	I	Timer1 External Input Pin
22	P5.6	I/O	General Purpose Digital I/O Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
	PWM0_CH6	O	PWM0 Channel6 Output Pin
	UART0_RXD	I	UART0 RX Pin
23	P5.7	I/O	General Purpose Digital I/O Pin
	I2C0_SDA	I/O	I2C0 Data Pin
	PWM0_CH7	O	PWM0 Channel7 Output Pin
	UART0_TXD	O	UART0 TX Pin
24	P2.2	I/O	General Purpose Digital I/O Pin
	UART2_TXD	O	UART2 TX Pin
	PWM0_CH0	O	PWM0 Channel0 Output Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
25	P2.3	I/O	General Purpose Digital I/O Pin
	UART2_RXD	I	UART2 RX Pin
	PWM0_CH1	O	PWM0 Channel1 Output Pin
	I2C0_SDA	I/O	I2C0 Data Pin
26	P2.4	I/O	General Purpose Digital I/O Pin
	UART1_RXD	I	UART1 RX Pin

	PWM0_CH2	O	PWM0 Channel2 Output Pin
27	P2.5	I/O	General Purpose Digital I/O Pin
	UART1_TXD	O	UART1 TX Pin
	PWM0_CH3	O	PWM0 Channel3 Output Pin
28	P2.6	I/O	General Purpose Digital I/O Pin
	SPI0_SS	O	SPI0 SS Pin
	PWM0_CH4	O	PWM0 Channel4 Output Pin
29	P4.6	I/O	General Purpose Digital I/O Pin
	ICE_CLK	I	ICE Clk Input Pin
	UART1_RXD	I	UART1 RX Pin
	I2C0_SCL	I/O	I2C0 CLK Pin
30	P4.7	I/O	General Purpose Digital I/O Pin
	ICE_DAT	I	Debug and Program Data Pin
	UART1_TXD	O	UART1 TX Pin
	I2C0_SDA	I/O	I2C0 Data Pin
31	-	-	-
32	-	-	-
33	XC1	AI	Crystal Pin1
34	XC2	AO	Crystal Pin2
35	-	-	-
36	GND	P	Ground Pin
37	ANT	AIO	Antenna Pin
38	-	-	-
39	VDD	P	Soc Power Supply VDD Pin
40	GND	P	Ground Pin
41	GND	P	Ground Pin

4 Electrical Characteristics

All the parameters are accurate to the one decimal place.

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Symbol	Description	Parameter			Unit
		Min	Typ	Max	
VDD	VDD1/VDD2	-0.3	-	3.6	V
V_I	Input Voltage	-0.3	-	VDD	V
V_O	Output Voltage	VSS	-	VDD	V
T_{OP}	Operating Temperature	-40	-	85	℃
T_{STG}	Storage Temperature	-40	-	125	℃

Note: Exceeding one or more of the limiting values may cause permanent damage to PAN2025.

Caution: Electrostatic sensitive device, comply with protection rules when operating.

4.2 DC Electrical Characteristics

Table 4-2 Voltage and Current

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VDD1/VDD2	Power Supply	2.2	3	3.6	V	TA=25℃
VSS	Ground	-	0	-	V	-
$I_{DP\_SLP\_RC}$	Deep sleep current	30	60	-	uA	MCU power down, SRAM maintain, HCLK off, 32K RC on
I_{ST_M0}	Standby Current	-	0.2	-	uA	External interrupts, CPU Power Down
I_{ST_M1}	Standby Current	-	1	-	uA	External interrupts, CPU Power Down, SRAM retention
I_{ST_M2}	Standby Current	-	2.5	-	uA	Sleep timer running, CPU Power Down
I_{ST_M3}	Standby Current	-	3.3	-	uA	Sleep timer running, CPU Sleep, SRAM retention
$I_{TX,0dBm}$	Operating Current of TX mode	-	50	-	mA	0dBm output power
$I_{TX,8dBm}$	Operating Current of TX mode	-	66	-	mA	8dBm output power
$I_{TX,10dBm}$	Operating Current of TX mode	-	68	-	mA	10dBm output power
I_{RX}	Operating Current of RX mode	-	40	-	mA	Maximum LNA gain
V_{OH}	Output High Level Voltage	VDD-0.3	-	VDD	V	-
V_{OL}	Output Low Level Voltage	VSS	-	VSS+0.3	V	-
V_{IH}	Input High Level Voltage	2.0	3	3.6	V	-
V_{IL}	Input Low Level Voltage	VSS	-	VSS+0.3	V	-

4.3 16 MHz Crystal Oscillator Characteristics

Table 4-3 16M RC Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{XTAL(16M)}$	Crystal Oscillator Frequency	-	-	16	-	MHz
ESR(16M)	Equivalent Series Resistance	-	-	-	80	Ω
$\Delta f_{XTAL(16M)}$	Crystal Frequency Tolerance	-	-20	-	20	ppm
$V_{CLK(EXT)(16M)}$	External Clock Voltage	-	0.1	0.8	-	V
φN(EXTERNAL)16M	Phase Noise	f_C = 50 kHz in case of an external reference clock	-	-	-130	dBc/Hz

4.4 Stable Low Frequency RCX Oscillator Characteristics

Table 4-4 Stable Low Frequency RCX Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{RC(RCX)}$	RCX Oscillator Frequency	Default setting,	-	40	-	Khz

4.5 AC Electrical Characteristics

Table 4-5 RF

Symbol	Condition	Min	Typ	Max	Unit
General frequency					
Fop	Operating Frequency	2400	-	2483	MHz
PLL_{res}	PLL Programming Resolution	-	1	-	MHz
F_{xtal}	Crystal Frequency	-	16	-	MHz
DR	Data Rate	-	1	-	Mbps
Transmitter					
PRF	Output Power	2	8	10	dBm
PRFC	Output Power Range	-16	-	-10	dBm
PBW	20dB Bandwidth for Modulated Carrier at 1Mbps	950	-	1100	MHz
MDR	Maximum Drift Rate	-	-	13	KHz/50us
FD	Frequency Deviation	200	-	300	KHz
Receiver					
RXmax	Maximum Received Signal at <0.1% BER	-	0	-	dBm
RXSENS	Sensitivity (0.1%BER) @1Mbps, GFSK	-	-91	-	dBm
C/ICO	C/I Co-channel Interference	-	14	-	dBc
C/I1M	Adjacent 1MHz Interference	-	2	-	dBc
C/I2M	Adjacent 2MHz Interference	-	-16	-	dBc
C/I≥3M	Adjacent ≥ 3MHz Interference	-	-26	-	dBc
C/Iimage	Image Frequency Interference	-	-12	-	dBc
C/Iimage±1M	Adjacent（1MHz）Interference to In-band Image Frequency	-	-35	-	dBc
P_IMD	Intermodulation Interference	-	-45	-	dBm

P_Blocking	Out-of-band Blocking Interference	-30	-	-	dBm

Table 4-6 DPLL

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD2	Power Supply	2.2	-	3.6	V	-
T_A	Temperature	-40	-	85	℃	-
F_{in}	Input Clock Frequency	-	16	-	MHz	-
F_{DPLL}	Clock Frequency	-	48	72	MHz	-

Table 4-7 ADC

Symbol	Parameter	Min	Typ	Max	Unit	Notes
-	Resolution	-	10	-	Bit	-
VDD2	Power Supply	2.5(for VTOP=2.4V) 2.2(for VTOP=1.4V)	-	3.6	VDDA	-
ITOT	Operation Current	880	-	1600	uA	-
INL	Integral Nonlinearity Error	-	-	±2	LSB	-
SYS_CLK	System Clock	-	-	48	MHz	-
Fadc	Clock Frequency	-	-	48	MHz	-
FS	Sample Rate	-	-	1.625	MHz	-
Ts	Sample Time	7	-	-	SYS_CLK	-
Th	Compare Time	25	-	-	SYS_CLK	-
TCONV	Data Output cycle	32	50	170	SYS_CLK	-
N	S-H counter	1	2	7	-	-
Vin	Analog input voltage	0 0	-	VDD/VDD-0.7 *Note2 2.0	V	-
Cin	Input Capacitance	-	10	-	pF	-
Rin	Input resistance	14.6	-	-	KΩ	See Note1
Vref	ADC reference voltage	-	VBG	-	V	-
DATA	ADC Output	000	-	FFF	HEX	-
SFDR	Spurious Free Dynamic range	-	64	-	dB	-

Note:

$$Rin = \frac{\text{EXTSMPT<9:0>(1+ADC\_CTL<19:16>)}}{f_{adc} \times C_{in} \times \ln \frac{V_{in}}{V_{in} - V_{real}}}$$

Note2:

- Input range ≥ 2V, 0 ~ VDD is recommended for PAN2025BX and PAN2025BY.
- Input range ≥ 2V, 0 ~ VDD-0.7 is recommended for PAN2025DX and PAN2025DY.

Table 4-8 LVR

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD2	Power Supply	2.2	3	3.6	V	-
VLVR	Threshold Voltage	-	1.9	-	V	-

Table 4-9 BOD

Symbol	Parameter	Vout(V) 1→0	Vout(V) 0→1	Test Conditions	Notes
V_{BOD}	Brown-Out Detector	2.0	2.1	EN_BOD=1 BODVL<2:0>=000	-
		2.2	2.3	EN_BOD=1 BODVL<2:0>=001	-
		2.5	2.6	EN_BOD=1 BODVL<2:0>=010	-
		2.7	2.8	EN_BOD=1 BODVL<2:0>=011	-
		3.0	3.1	EN_BOD=1 BODVL<2:0>=101	-

5 Reference Schematic Diagram

5.1 Application Reference Circuit for QFN32

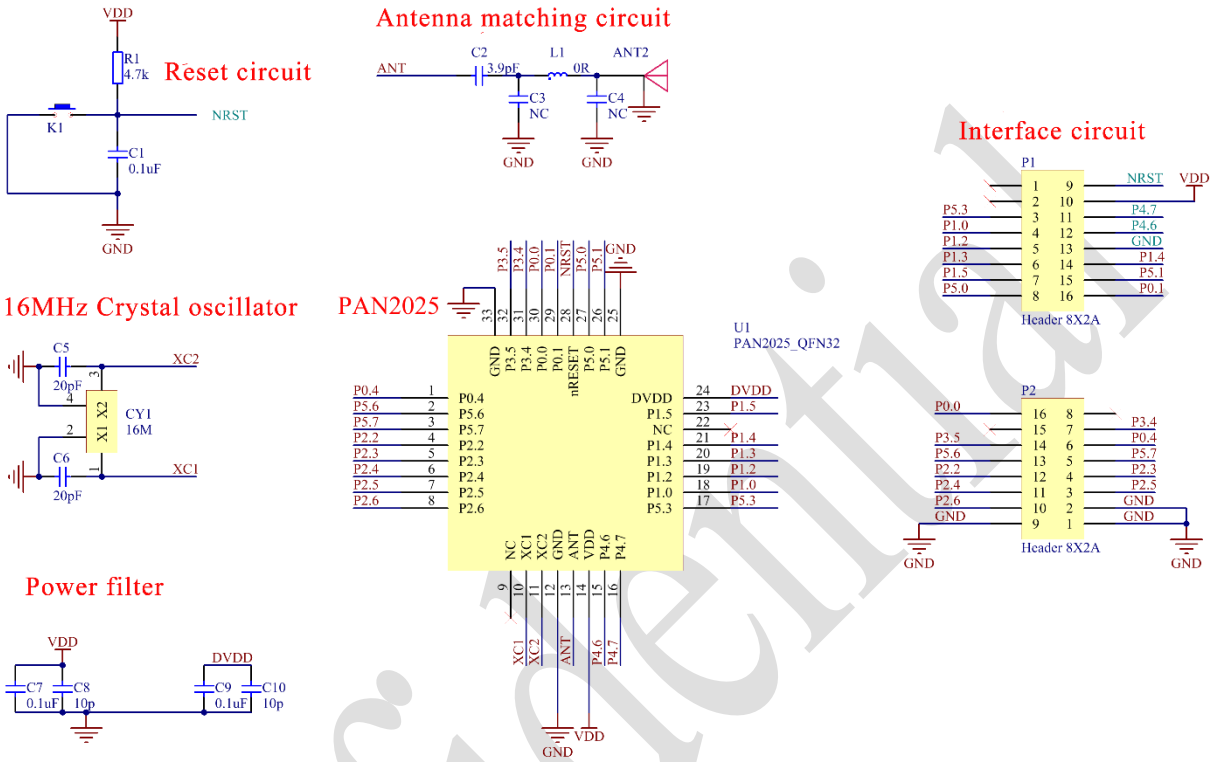

Figure 5-1 Application Reference Circuit for QFN32

5.2 Application Reference Circuit for QFN40

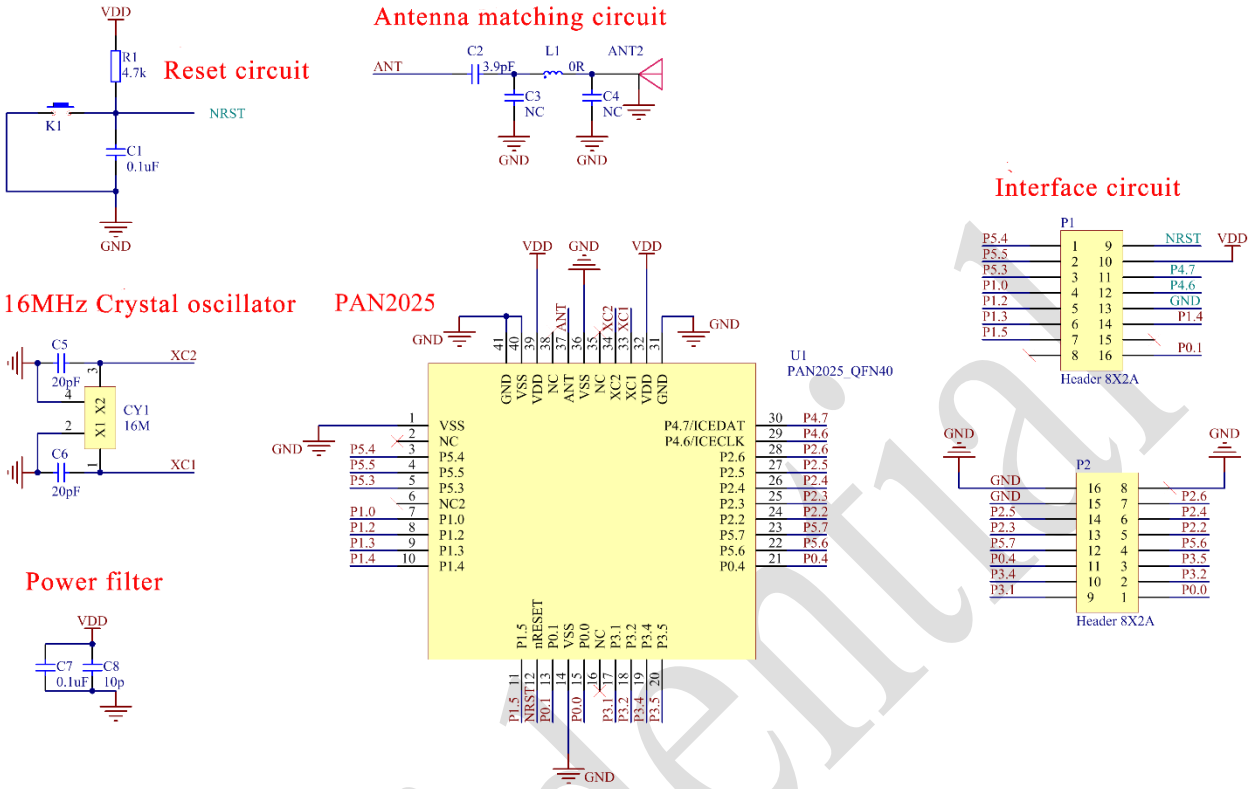

Figure 5-2 Application Reference Circuit for QFN40

6 Package Dimensions

6.1 Package Dimensions for QFN32

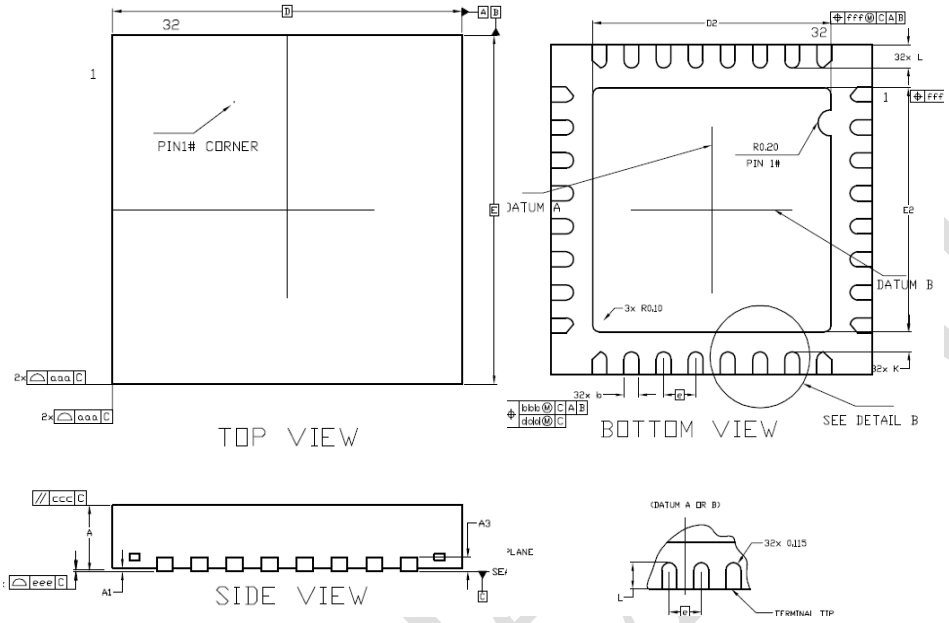

Figure 6-1 QFN32 Package Views

Table 6-1 QFN32 Package Detail Parameters

Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	0.70	0.75	0.80
	0.85	0.90	0.95
A1	0	0.02	0.05
A3	-	0.20 REF	-
b	0.18	0.23	0.28
D	5.00BSC		
E	5.00BSC		
D2	3.55	3.65	3.75
E2	3.55	3.65	3.75
e	0.50BSC		
L	0.30	0.35	0.40
K	0.20	-	-
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

6.2 Package Dimensions for QFN40

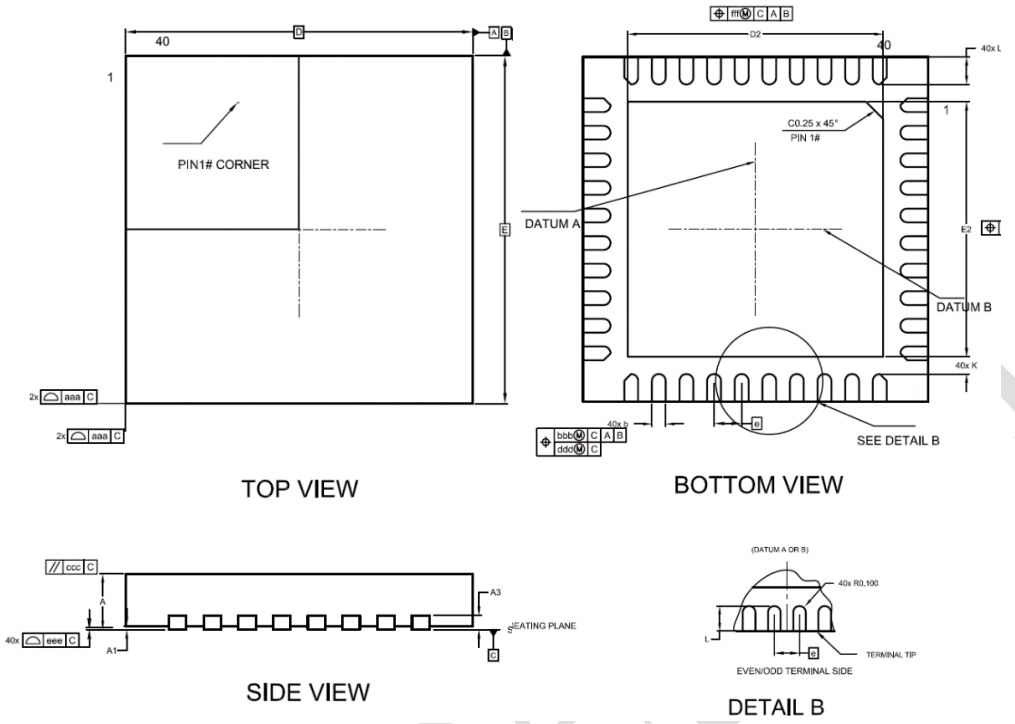

Figure 6-2 QFN40 Package Views

Table 6-2 QFN40 Package Detail Parameters

Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	0.70	0.75	0.80
	0.85	0.90	0.95
A1	0	0.02	0.05
A3	-	0.20REF	-
b	0.15	0.20	0.25
D	5.0BSC		
E	5.0BSC		
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.40BSC		
L	0.35	0.40	0.45
K	0.20	-	-
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

7 Precautions

(1) This product is a CMOS device and should be protected against static electricity during storage, transportation and use.

(2) Grounding when device is in use.

(3) Reflow temperature can not exceed 260℃.

8 Storage Conditions

(1) Products should be stored in sealed packages: when the temperature is less than 30 degrees and the humidity is less than 90%, it can last for 12 months.

(2) After the package is opened, the components will be used in the reflow process or other high-temperature processes. The following conditions must be met:

1) Completed within 72 hours and the factory environment is less than 30℃≤ 60% RH.

2) Stored in 10% RH environment.

3) Exhaust at 125℃ for 24 hours to remove internal water vapor before used.

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